Datasheet

Three-phase BLDC Motor Controller with Built-in Pre-driver

ET8061

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Contents

ET8061 Three-phase BLDC Motor Controller with Built-in Pre-driver

1 System Introduction

1.1 Overview

ET8061 is an IC with built-in pre-driver designed for three-phase BLDC motor driver applications. Due to a high level of integration, few peripheral components are required. The chip supports sensored SVPWM (ET8061L) and sensorless FOC to reduce audible noise and minimize torque ripple in motor drives. Motor parameters, startup control parameters and speed regulation mode can be configured via GUI, and are stored in built-in EEPROM. Analog voltage input, PWM or I^2C interface is available for motor speed regulation. Moreover, the chip integrates speed indicator to read motor speed in real time via FG/RD_SDA pin or I^2C interface. It is secured with a wide range of protection features, including over-current protection (OCP), current-limiting protection (CLP), under-voltage lockout (UVLO), temperature sensor detect (TSD), motor lock protection (MLP), configurable maximum speed protection, bus voltage protection, abnormal Hall input detection (HALLERR) protection (ET8061L), etc. The chip also supports power closed-loop control.

1.2 Applications

Air conditioner indoor units, air purifiers, water pumps, etc.

ET8061L

1.3 Features

- VCC range: 12V ~ 20V
- Sensorless FOC
- ET8061L supports sensor-based FOC (Hall-IC/Hall-Sensor)
- ET8061L supports sensor-based SVPWM (Hall-IC/Hall-Sensor)
- 6N pre-driver with configurable deadtime
- Drive current: +0.21A/-0.36A
- Constant speed control mode, constant current control mode or constant power control mode is optional.
- Forward and reverse direction control
- FG and RD output
- PWM, analog voltage input or I^2C interface for motor speed regulation
- Support multi-stage lead angle curve to fit motor characteristics
- Soft-on and soft-off features protect the motor from abrupt startup and reduces current shock and noise
- Support protection features, including OCP, CLP, UVLO, TSD, MLP, configurable maximum speed protection, bus voltage protection, abnormal Hall input detection (HALLERR) protection (ET8061L), etc.

ET8061T

1.4 Typical Application Diagram

1.4.1 ET8061L in Sensor-based SVPWM Mode

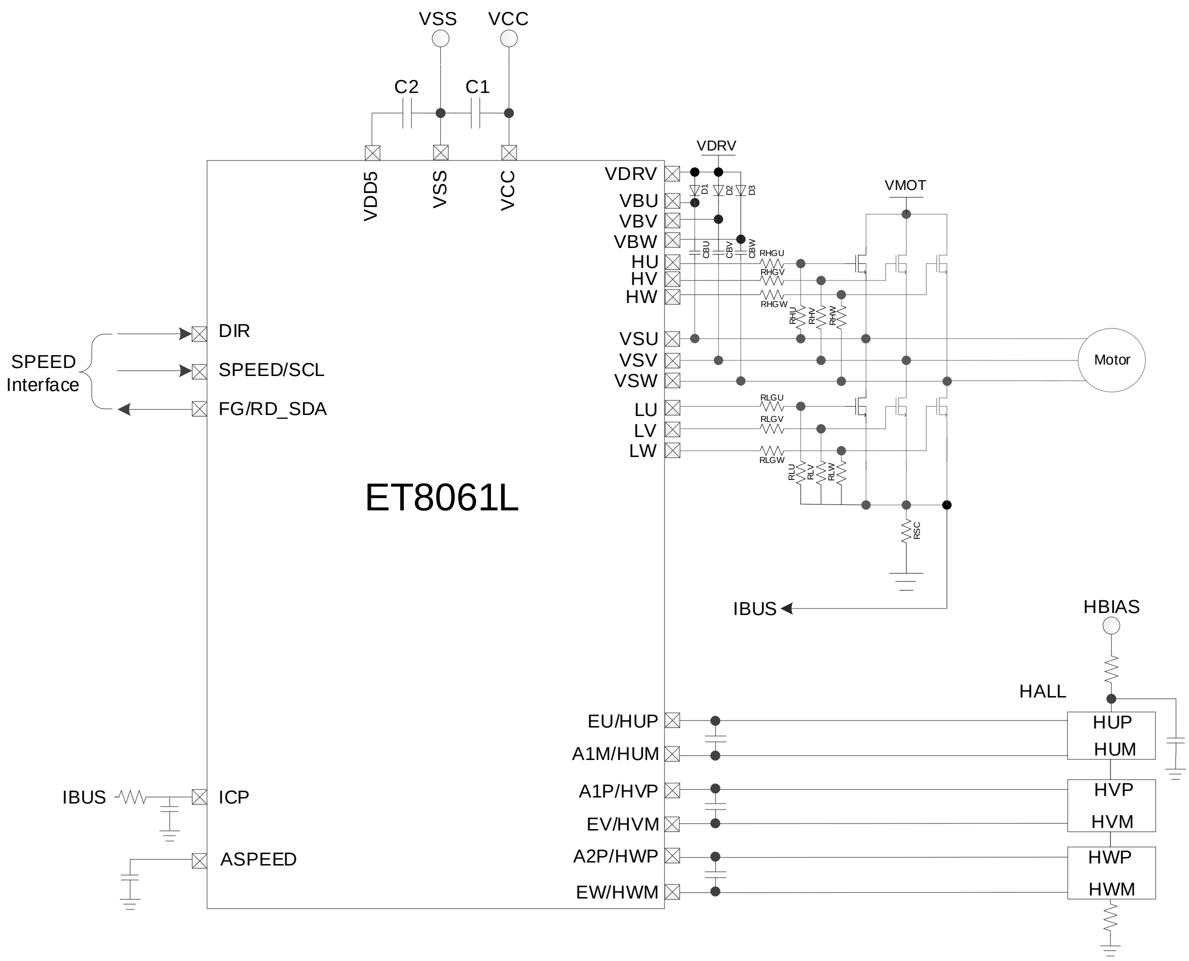


Figure 1-1 ET8061L in Sensor-based SVPWM Mode

1.4.2 ET8061L in Sensorless FOC Mode with Dual/Triple-shunt Current Sampling

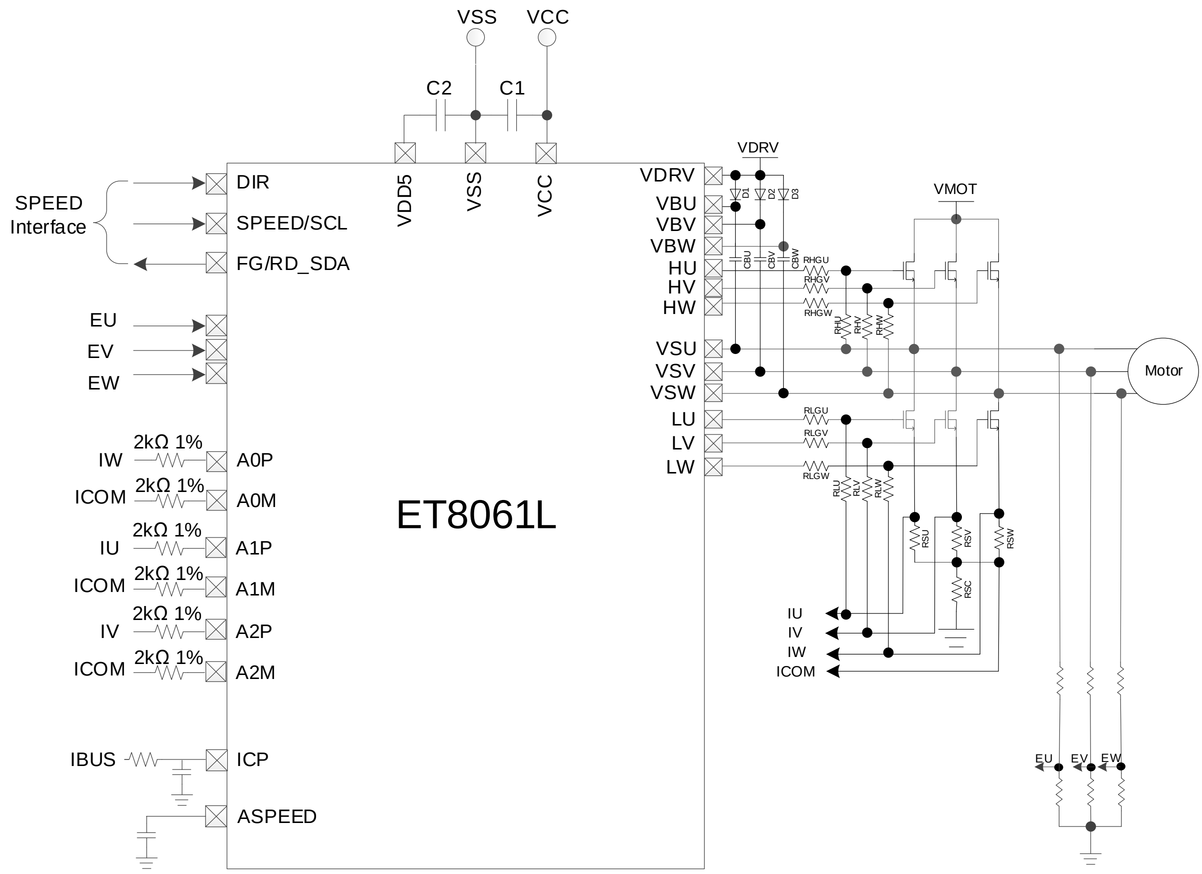


Figure 1-2 ET8061L in Sensorless FOC Mode with Dual/Triple-shunt Current Sampling

1.4.3 ET8061L in Sensorless FOC Mode with Single-shunt Current Sampling

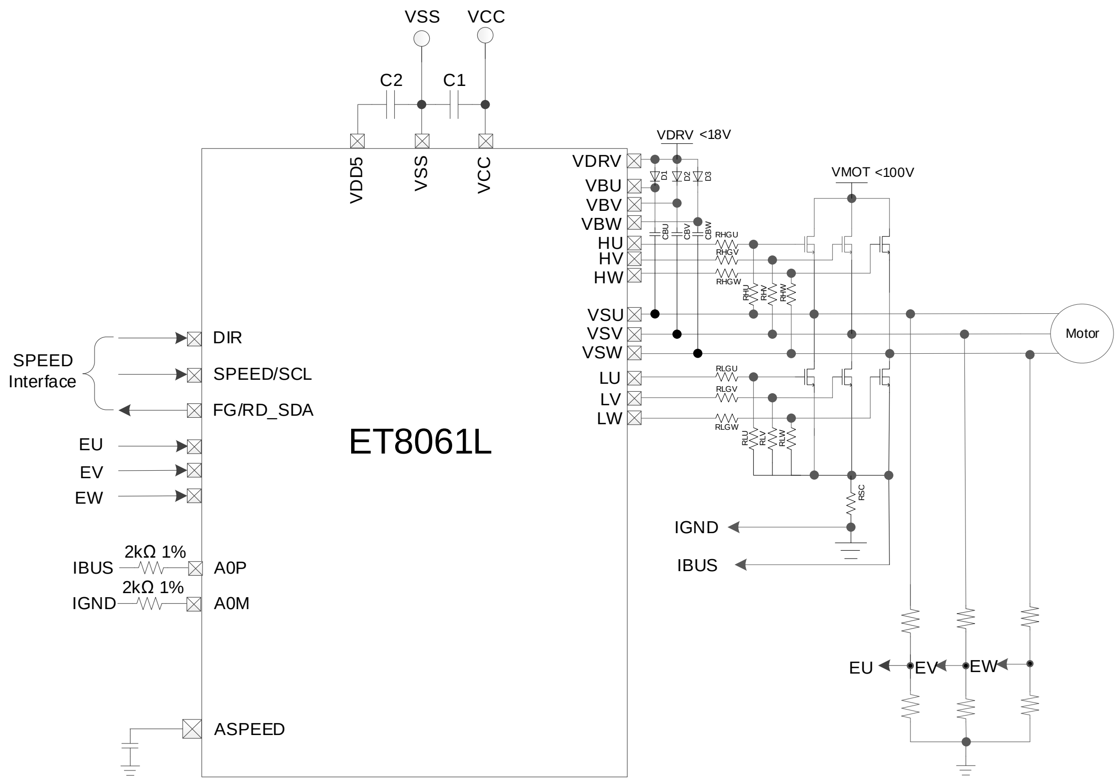


Figure 1-3 ET8061L in Sensorless FOC Mode with Single-shunt Current Sampling

1.4.4 ET8061T in Sensorless FOC Mode with Dual-shunt Current Sampling

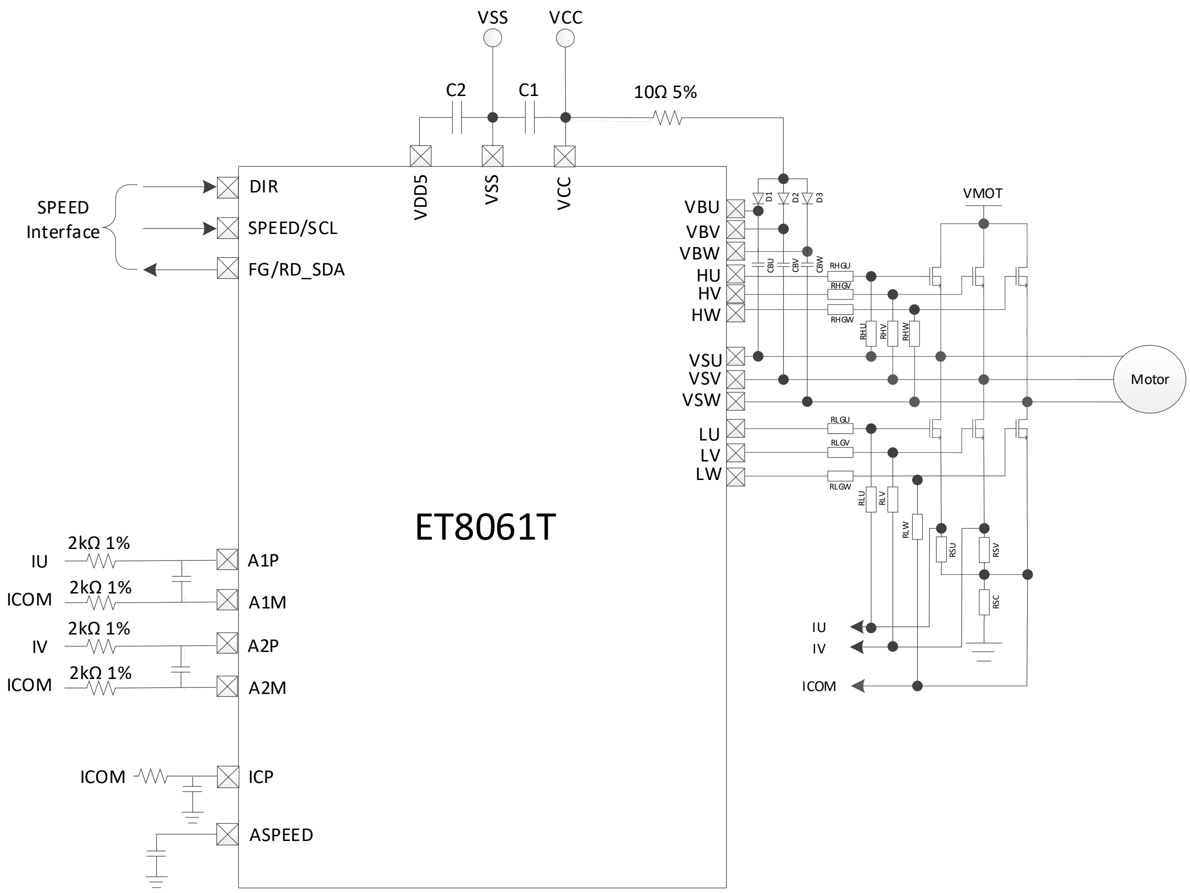


Figure 1-4 ET8061T in Sensorless FOC Mode with Dual-shunt Current Sampling

1.5 Functional Block Diagram

1.5.1 ET8061L

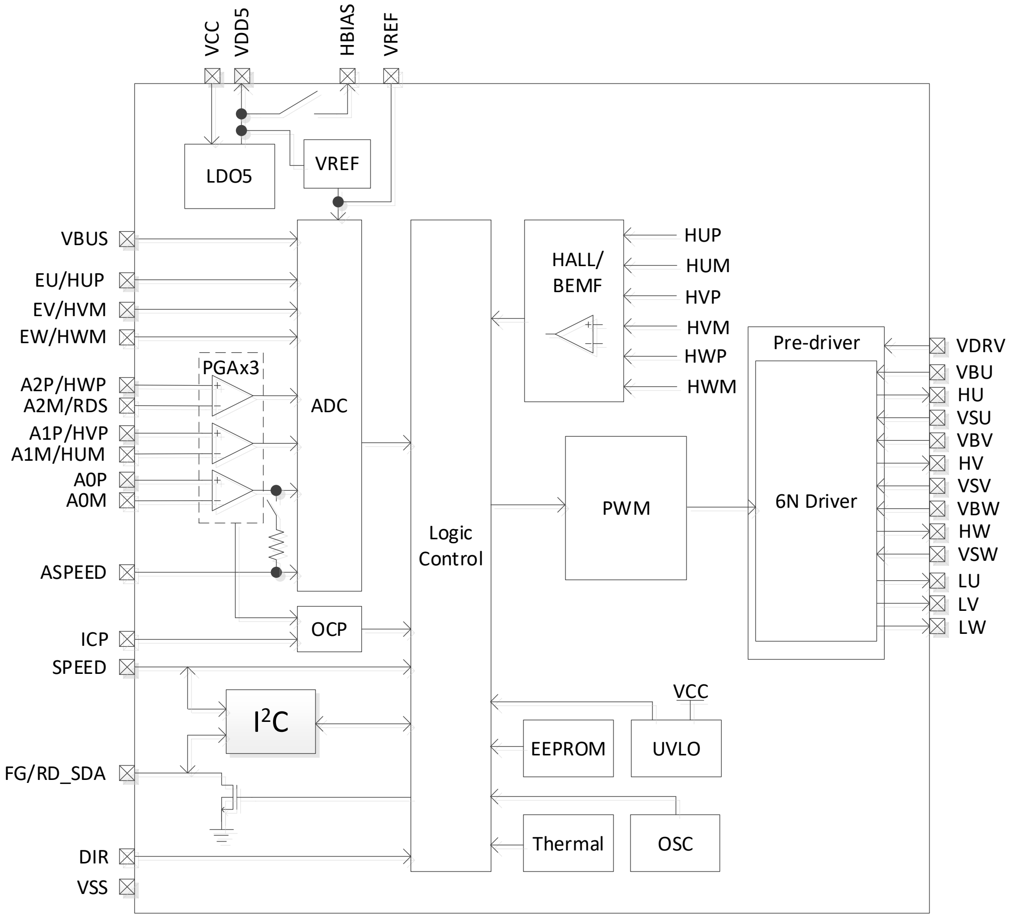


Figure 1-5 Functional Block Diagram of ET8061L

1.5.2 ET8061T

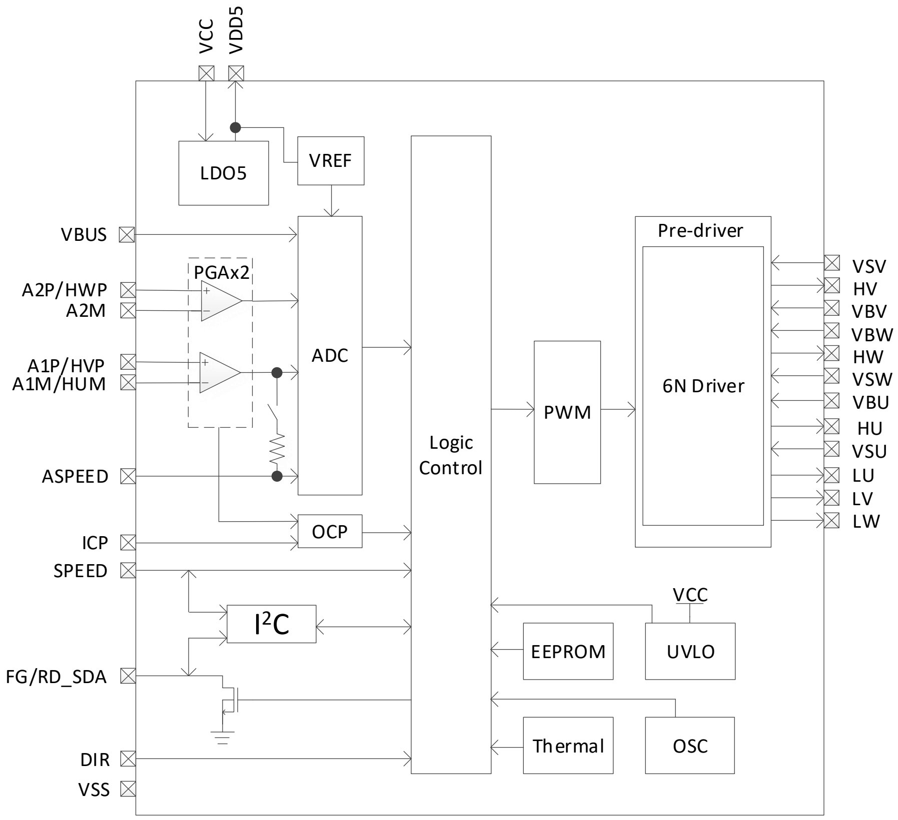


Figure 1-6 Functional Block Diagram of ET8061T

1.6 Pinout Diagram

1.6.1 ET8061L LQFP48

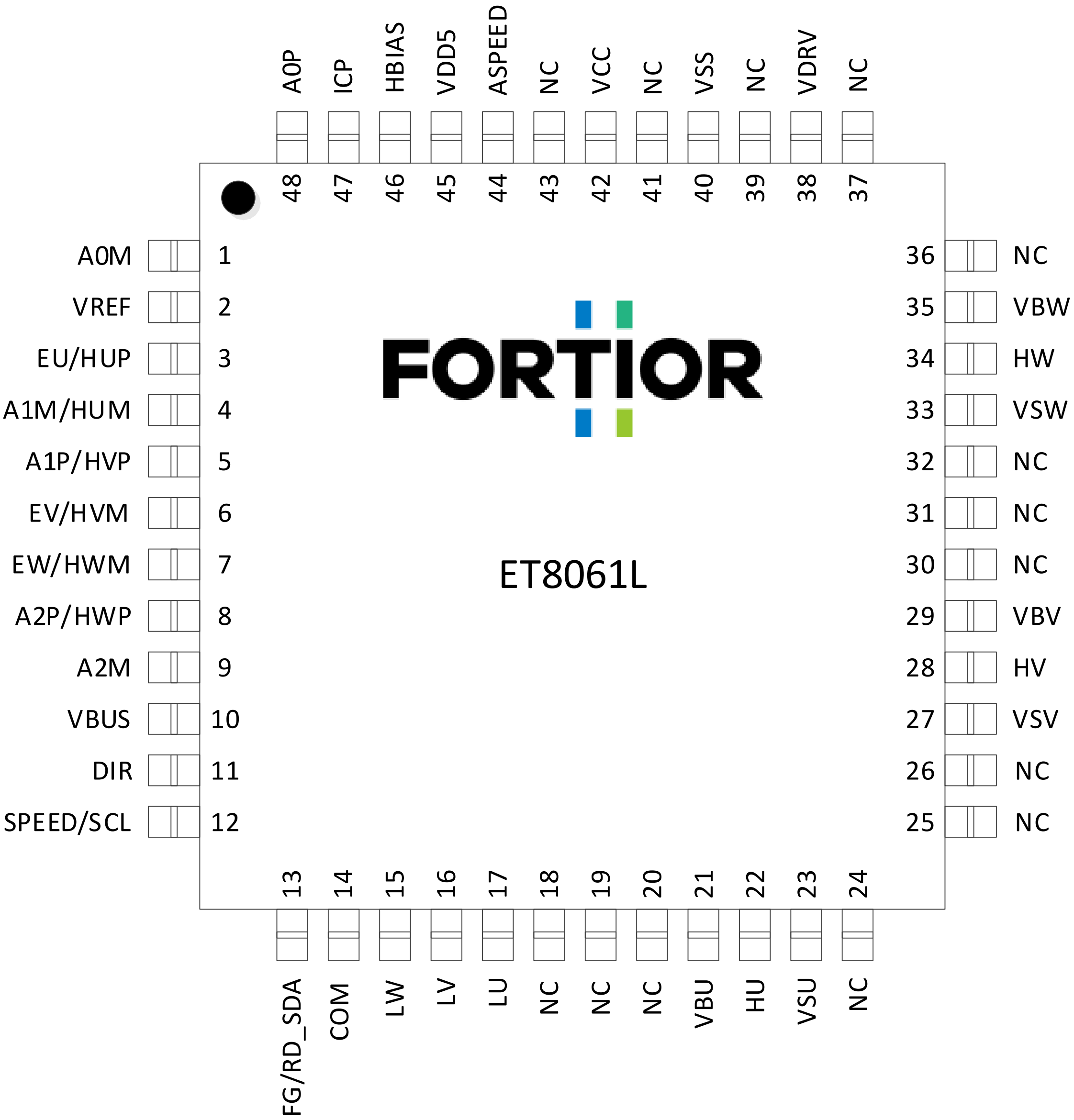


Figure 1-7 ET8061L LQFP48_7X7 Pinout Diagram

1.6.2 ET8061T TSSOP28

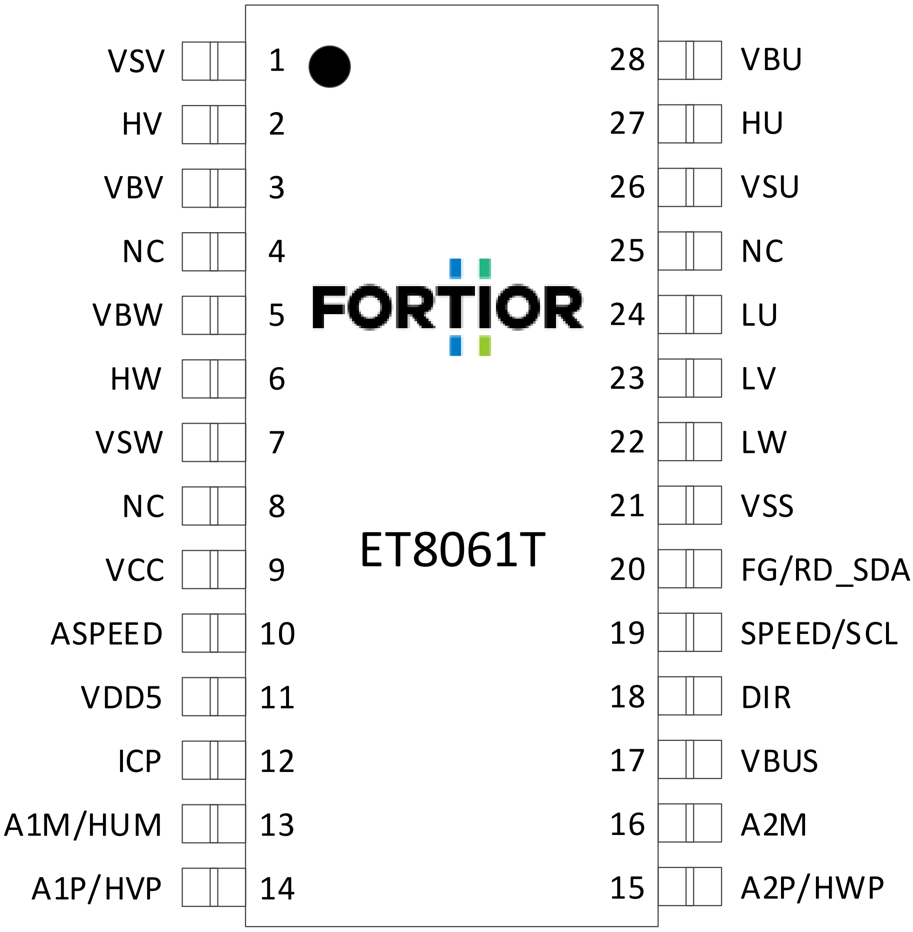


Figure 1-8 ET8061T TSSOP28_9.7X4.4 Pinout Diagram

1.7 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

1.7.1 ET8061L LQFP48 Pins

Table 1-1 ET8061L LQFP48 Pin Descriptions

Pin	ET8061L LQFP48	IO Type	Description
A0M	1	AI	AMP0 negative input
VREF	2	AO	ADC reference voltage output, with a 1μF external capacitor connected to ground
EU/ HUP	3	AI/ AI	U-phase BEMF voltage input Positive input of U-phase differential Hall sensor or input of U-phase Hall IC
A1M/ HUM	4	AI/ AI	AMP1 negative input Positive input of U-phase differential Hall sensor
A1P/ HVP	5	AI/ AI	AMP1 positive input Positive input of V-phase differential Hall sensor
EV/ HVM	6	AI/ AI	V-phase BEMF voltage input Negative input of V-phase differential Hall sensor or input of V-phase Hall-IC
EW/ HWM	7	AI/ AI	W-phase BEMF voltage input Negative input of W-phase differential Hall sensor or input of W-phase Hall IC
A2P/ HWP	8	AI/ AI	AMP2 positive input Positive input of W-phase differential Hall sensor
A2M	9	AI	AMP2 negative input
VBUS	10	AI	VDC bus voltage input after voltage division
DIR	11	DI	Motor rotation control, with built-in pull-up resistor 1: Forward rotation. U --> V --> W. 0: Reverse rotation. U --> W --> V.
SPEED/ SCL	12	DI/ DB	Speed control input; PWM speed regulation I^2C SCL
FG/ RD_SDA	13	DO/ DB	Motor speed signal or motor block indication, with collector open-drain output I^2C SDA, configured as collector open-drain output
COM	14	P	Pre-driver ground
LW	15	DO	6N pre-driver low-side W-phase PWM output
LV	16	DO	6N pre-driver low-side V-phase PWM output
LU	17	DO	6N pre-driver low-side U-phase PWM output
NC	18		Not connected
NC	19		Not connected
NC	20		Not connected
VBU	21	P	6N pre-driver high-side U-phase bootstrap power supply
HU	22	DO	6N pre-driver high-side U-phase PWM output
VSU	23	P	6N pre-driver U-phase input, as GND reference for U-phase high-side bootstrap

Pin	ET8061L LQFP48	IO Type	Description
NC	24		Not connected
NC	25		Not connected
NC	26		Not connected
VSV	27	P	6N pre-driver V-phase input, as GND reference for V-phase high-side bootstrap
HV	28	DO	6N pre-driver high-side V-phase PWM output
VBV	29	P	6N pre-driver high-side V-phase bootstrap power supply
NC	30		Not connected
NC	31		Not connected
NC	32		Not connected
VSW	33	P	6N pre-driver W-phase input, as GND reference for W-phase high-side bootstrap
HW	34	DO	6N pre-driver high-side W-phase PWM output
VBW	35	P	6N pre-driver high-side W-phase bootstrap power supply
NC	36		Not connected
NC	37		Not connected
VDRV	38	P	6N pre-driver power supply, 8V~18V, with an external 1μF ~ 10μF capacitor
NC	39		Not connected
GND	40	P	Ground
NC	41		Not connected
VCC	42	P	VCC
NC	43		Not connected
ASPEED	44	AI	Analog voltage input for motor speed regulation
VDD5	45	P	5V LDO output
HBIAS	46	DO	Hall bias power supply, internally connected to VDD5 via a switch
ICP	47	AI	Over-current detection input
A0P	48	AI	AMP0 positive input

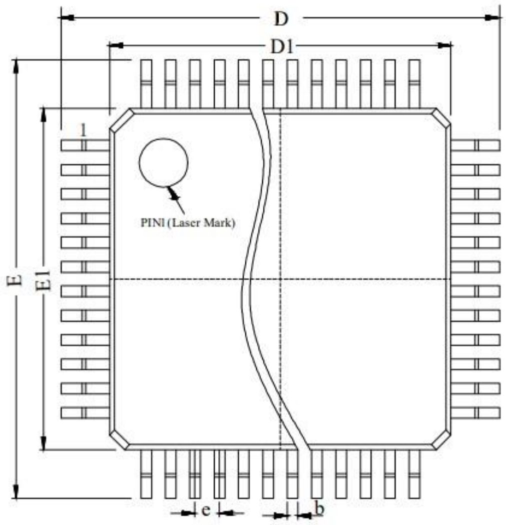
1.7.2 ET8061T TSSOP28 Pins

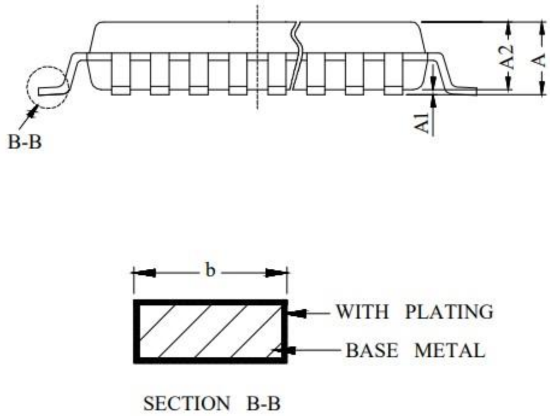
Table 1-2 ET8061T TSSOP28 Pin Descriptions

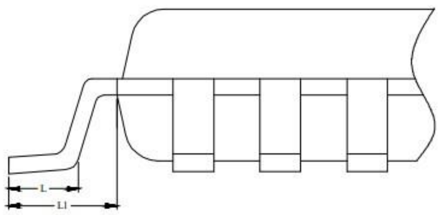
Pin	ET8061T TSSOP28	IO Type	Description
VSV	1	P	6N pre-driver V-phase input, as GND reference for V-phase high-side bootstrap
HV	2	DO	6N pre-driver high-side V-phase PWM output
VBV	3	P	6N pre-driver high-side V-phase bootstrap power supply
NC	4		Not connected
VBW	5	P	6N pre-driver high-side W-phase bootstrap power supply
HW	6	DO	6N pre-driver high-side W-phase PWM output
VSW	7	P	6N pre-driver W-phase input, as GND reference for W-phase high-side bootstrap
NC	8		Not connected
VCC	9	P	VCC
ASPEED	10	AI	Analog voltage input for motor speed regulation
VDD5	11	P	5V LDO output
ICP	12	AI	Over-current detection input
A1M/ HUM	13	AI/ AI	AMP1 negative input Positive input of U-phase differential Hall sensor
A1P/ HVP	14	AI/ AI	AMP1 positive input Positive input of V-phase differential Hall sensor
A2P/ HWP	15	AI/ AI	AMP2 positive input Positive input of W-phase differential Hall sensor
A2M	16	AI	AMP2 negative input
VBUS	17	AI	VDC bus voltage input after voltage division
DIR	18	DI	Motor rotation control, with built-in pull-up resistor 1: Forward rotation. U --> V --> W. 0: Reverse rotation. U --> W --> V.
SPEED/ SCL	19	DI/ DB	Speed control input; PWM speed regulation I^{2}C SCL
FG/ RD_SDA	20	DO/ DB	Motor speed signal or motor block indication, with collector open-drain output I^{2}C SDA, configured as collector open-drain output
VSS	21	P	Ground
LW	22	DO	6N pre-driver low-side W-phase PWM output
LV	23	DO	6N pre-driver low-side V-phase PWM output
LU	24	DO	6N pre-driver low-side U-phase PWM output
NC	25		Not connected
VSU	26	P	6N pre-driver U-phase input, as GND reference for U-phase high-side bootstrap
HU	27	DO	6N pre-driver high-side U-phase PWM output
VBU	28	P	6N pre-driver high-side U-phase bootstrap power supply

2 Package Information

2.1 ET8061L LQFP48_7X7



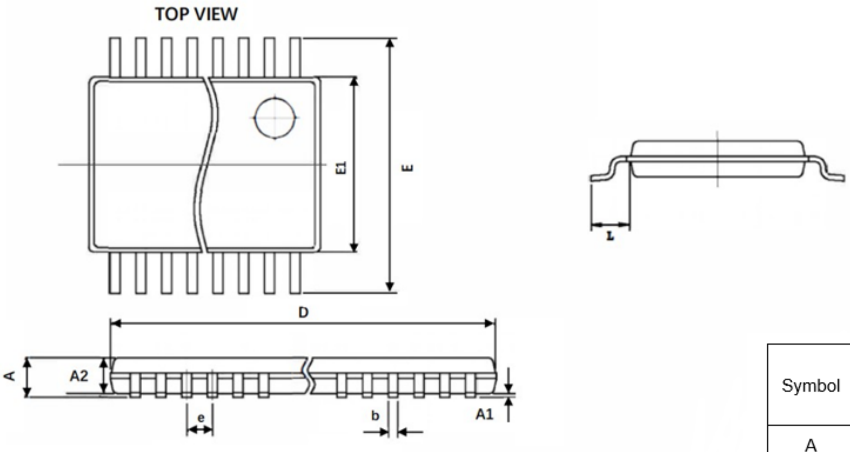




LQFP48			
SYMBOL	MILLIMETER		
	MIN	SPEC	MAX
A			1.6
A1	0.05	0.1	0.15
A2	1.35	1.4	1.45
E	8.8	9	9.2
D	8.8	9	9.2
E1	6.9	7	7.1
D1	6.9	7	7.1
L1		1	
L	0.45		0.8
e		0.5	
b	0.18		0.27

Figure 2-1 ET8061L LQFP48_7X7 Package Drawings and Dimensions

2.2 ET8061T TSSOP28_9.7X4.4



Symbol	Description	TSSOP28	
		Min.	Max.
A	Total Height		1.2
A1	Height between Base Plane and Setting Plan	0.1	0.15
A2	Package Height	0.8	1.05
E	Total Width	6.2	6.6
E1	Package Width	4.3	4.5
D	Package Length	9.6	9.8
L	Pin Length		1
e	Pin Spacing	0.65	
b	Pin Width	0.2	0.3

Figure 2-2 ET8061T TSSOP28_9.7X4.4 Package Drawings and Dimensions

3 Ordering Information

Table 3-1 Model Selections

Model	Power Supply (V)		Driver Interface	Control Features						Protection Features							Operating Temperature T_j(℃)	Lead-free	Package
	VCC	VDRV		Driver Type	Speed Regulation			Forward and Reverse Rotation	Initial Position Detection	OCP/CLP	UVLO	OVLO	MLP	HALLERR	TSD	Phase Loss Protection			
					I^2C	PWM	Analog Voltage												
ET8061L	12 ~ 20	10 ~ 20	6N Pre-driver	Sensored/ Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	√	√	-40 ~ 150	√	LQFP48 (7X7mm)
ET8061T	12 ~ 20	-	6N Pre-driver	Sensorless Sine-wave	√	√	√	√	-	√	√	√	√	-	√	√	-40 ~ 150	√	TSSOP28 (9.7X4.4mm)

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

(T_A = 25°C and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Ambient Temperature T_A		-40	-	85	°C
Operating Junction Temperature T_J		-40	-	150	°C
Storage Temperature		-55	-	150	°C
VCC to VSS Voltage		-0.3	-	30	V
VDD5 to VSS Voltage		-0.3	5	6.5	V
VDRV to VSS Voltage		-0.3	-	25	V
High-side Floating Absolute Voltage $V_{BU,BV,BW}$		-0.3	-	625	V
High-side Floating Offset Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 25	-	$V_{BU,BV,BW}$ + 0.3	V
High-side Output Voltage $V_{HU,HV,HW}$		$V_{SU,SV,SW}$ - 0.3	-	$V_{BU,BV,BW}$ + 0.3	V
Low-side Output Voltage $V_{LU,LV,LW}$		-0.3	-	V_{DRV} + 0.3	V
Other IOs to VSS Voltage		-0.3	-	VDD5 + 0.3	V

Note: Stress values greater than "Absolute Maximum Ratings" listed above may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

4.2 Global Electrical Characteristics

Table 4-2 Global Electrical Characteristics

(T_A = 25°C and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage		12	-	20	V
VDD5 Operating Voltage		3	-	5.5	V
VDRV Operating Voltage		10	-	20	V
$V_{BU,BV,BW}$ Floating Voltage		-	-	600	V
$V_{BU,BV,BW}$ to $V_{SU,SV,SW}$ Voltage		-	-	20	V
System Clock Rate		23.5	24	24.5	MHz
I_{VCC} Operating Current		-	15	25	mA
I_{VCC} Standby Current		5	7	10	mA
I_{VCC} Sleep-mode Current		-	50	100	µA
VBS UVLO Lockout Voltage		7.2	8.1	9.0	V
VBS UVLO Release Voltage		7.8	8.7	9.6	V
VCC Release Voltage V_{CCUVH}		11.5	12.1	12.7	V
VCC Lockout Voltage V_{CCUVL}		10.5	11.1	11.7	V

4.3 IO Electrical Characteristics (DIR/SPEED/FG)

Table 4-3 IO Electrical Characteristics (DIR/SPEED/FG)

(T_A = 25°C and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage V_{IH}		0.7*VDD5	-	-	V
Low-level Input Voltage V_{IL}		-	-	0.2*VDD5	V
SPEED/DIR/A1P Pull-up Resistor		-	33	-	kΩ
SPEED Pull-down Resistor		-	22	-	kΩ
EW/EV/EU/A2M Pull-up Resistor		-	5.6	-	kΩ
V_{OH} DRV High-level Output Voltage	I_O = 20mA	-	0.7	-	V
V_{OL} DRV Low-level Output Voltage	I_O = 20mA	-	0.2	-	V
I_{OH} DRV High-level Output Short-circuit Pulsed Current	V_O = 0V	-	0.21	-	A
I_{OL} DRV Low-level Output Short-circuit Pulsed Current	V_O = 15V	-	0.36	-	A

4.4 PWM/CLOCK Input Frequency

Table 4-4 PWM/CLOCK Input Frequency

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWM Input Frequency		100	-	100k	Hz
CLOCK Input Frequency		20	-	1400	Hz

4.5 6N Pre-driver Electrical Characteristics

Table 4-5 6N Pre-driver Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Peak Output Current		-	0.21	-	A
Low-level Peak Output Current		-	0.36	-	A
VCC Supply Voltage		12	-	20	V
High-side Floating Voltage $V_{BU,BV,BW}$		-	-	600	V
High-side Floating Voltage $V_{SU,SV,SW}$		$V_{BU,BV,BW}$ - 20	-	$V_{BU,BV,BW}$ - 11	V
VDRV UVLO Threshold Voltage		8.1	9	9.9	V
VDRV UVLO Release Voltage		7.5	8.4	9.3	V
VDRV UVLO Hysteresis Voltage		0.4	0.6	-	V
Output Rise Time	1nF load, from 10% to 90%	-	90	-	ns
Output Fall Time	1nF load, from 90% to 10%	-	50	-	ns
Deadtime	DT	-	500	-	ns

4.6 Speed Control with Analog Voltage

Table 4-6 Speed Control with Analog Voltage

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ASPEED Input Voltage		0	-	VDD5	V

4.7 Package Thermal Resistance

Table 4-7 LQFP48 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Temperature Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	36	°C/W
	JEDEC standard, 1S0P PCB	60	°C/W
Junction-to-case Temperature Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	10.5	°C/W

Table 4-8 TSSOP28 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Temperature Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	64	°C/W
	JEDEC standard, 1S0P PCB	81	°C/W
Junction-to-case Temperature Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	19	°C/W

Note: The actual measurements may vary depending on the conditions.

5 Function Description

5.1 VREF

VREF is applied to internal digital logic and analog circuits only, and cannot be used for external circuits. A capacitor of 1μF or above shall be added at VREF pin to stabilize the power supply.

5.2 HBIAS (ET8061L)

HBIAS is Hall bias power supply which is internally connected to VDD5 through a configurable switch. The maximum load capacity is 10mA. In sleep mode, the switch is open to cut off the power supplied to Hall sensors.

5.3 DIR

Forward or reverse direction control (DIR) pin is used to reverse motor rotation by changing the DIR level. Pull-ups make the pin state as "High" (or "1") by default.

5.4 ASPEED

Analog voltage for motor speed regulation (ASPEED) pin is used to input analog voltage for speed regulation.

5.5 SPEED

Speed control (SPEED) pin is used to input duty cycle for speed regulation depending on the settings. In addition, SPEED pin serves as the clock line (SCL) for I^2C communication.

5.6 FG/RD_SDA

Speed detection and fault indication (FG/RD_SDA) pin is an open-drain output. When this pin is set to FG, it outputs speed feedback signal to indicate rotation speed of the motor, and when it is set to RD, it outputs high-level signal to indicate the fault state. In addition, the pin serves as the data line (SDA) for I^2C communication.

Configuring FG/RD_SDA to FG outputs FG signal, that is, FG/RD_SDA pin is selected to output FG signal. The output frequency of FG signal is determined by FGDIV (frequency division coefficient) and FGMUL (frequency multiplication coefficient). FGMUL can be set as 1, 3, 4 and 12, while FGDIV as 1, 1/3, 1/4 and 1/5. k (coefficient of output frequency) = FGMUL*FGDIV.

Table 5-1 FG Configurations

Coefficient of Output Frequency (k)		**FGMUL**			
		1	**3**	**4**	**12**
FGDIV	**1**	1	3	4	12
	1/3	1/3	3/3	4/3	12/3
	1/4	1/4	3/4	4/4	12/4
	1/5	1/5	3/5	4/5	12/5

The number of FG signals in one mechanical cycle is equal to pp*k (pp refers to pole-pair number of the motor).

Example: For a 4-pole-pair motor, if FGMUL is set as 3 and FGDIV as 1/4, that is, k = 3/4, three FG signals are displayed in one mechanical cycle (4 * 3/4).

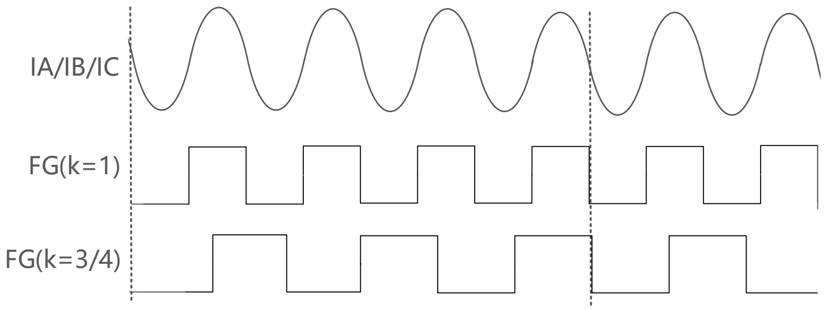


Figure 5-1 FG Output Waveforms at k = 1 and k= 3/4

In sensored mode, if FG3 or FG1 frequency multiplication to follow Hall output is configured, FG signals are output based on the corresponding settings. Otherwise, FG signals are output based on the configured FGDIV and FGMUL.

5.7 Speed Control

5.7.1 Speed Control Modes

The chip supports three types of speed control input interface: PWM, analog voltage and I^2C, and only one of them can be chosen at a time. If analog voltage is selected, voltage value input to the ASPEED pin controls the speed; if PWM is selected, duty cycle of PWM input to SPEED pin controls the speed, and if I^2C is selected, SPEED pin serves as the clock line (SCL) and FG/RD_SDA pin as the data line (SDA).

5.7.2 Speed Control Curve

The control waveform is presented as below, where x-coordinate refers to the duty cycle of PWM input (In I^2C control and analog control modes, the input can be converted to the corresponding PWM duty cycle.), and y-coordinate refers to the output duty cycle, which represents different physical quantities in different control modes.

The speed control curve is configured by setting the output duty cycle at the start and end points. The start point is determined by X_ON and Y_ON, and the end point by X_Max and Y_Max. The output of other points between them increases linearly as the input varies.

The y-coordinate represents Duty in voltage-loop control mode; Speed in speed-loop control mode; and Current in current-loop control mode.

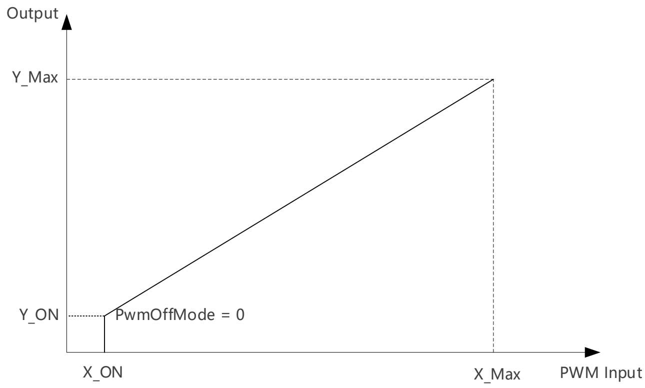


Figure 5-2 Output Curve in Speed-loop or Current-loop Mode (PwmOffMode = 0)

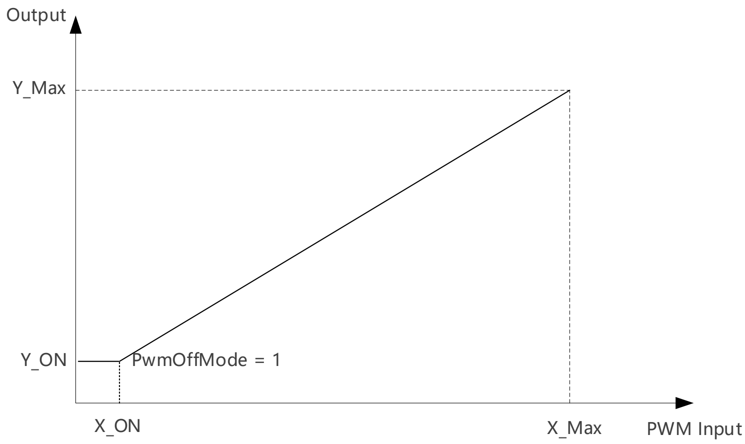


Figure 5-3 Output Curve in Speed-loop or Current-loop Mode (PwmOffMode = 1)

5.8 Lead Angle Curve

In sensored SVPWM control mode, lead angle curve corresponding to duty cycle of the voltage output is shown in Figure 5-4, where x-coordinate denotes duty cycle of the PWM voltage and y-coordinate represents the lead angle. The multi-stage lead angle curve is developed by setting lead angle at 9 points, which better fits the motor characteristics. Such 9 points are 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, 87.5% and 100%, respectively, and the maximum angle difference between each two adjacent points is 10.547°.

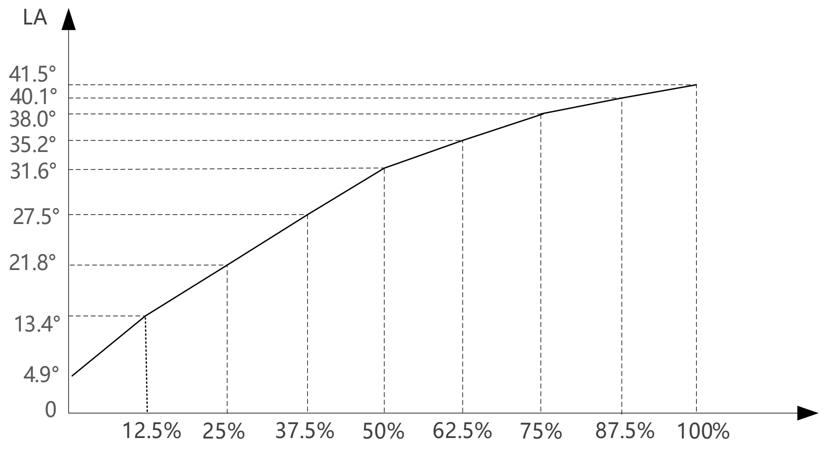


Figure 5-4 Lead Angle Curve

5.9 Sleep Mode

The motor enters sleep mode in 6s after ASPEED is set to 0V and SPEED pin is connected to GND.

Wakeup conditions: In I^2C speed control mode, the chip exits sleep mode after receiving the matched I^2C ID. In PWM speed control mode, the chip exits sleep mode when a high-level voltage is input to SPEED pin. In analog voltage control mode, the chip exits sleep mode when the voltage of ASPEED pin is greater than 1.5V or when a high-level voltage is input to SPEED pin.

5.10 Soft-on and Soft-off

Soft-on feature gradually increases the current during start-up process, and soft-off feature gradually decreases the current during shut-down process. The two features protect the motor from abrupt startup or shutdown and reduce noise during operation.

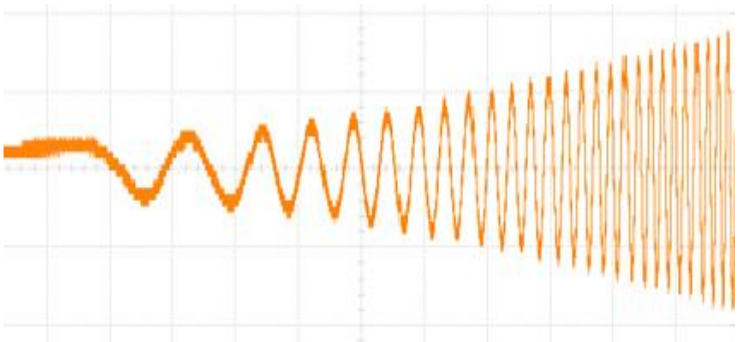


Figure 5-5 Soft-on Phase Current Waveform

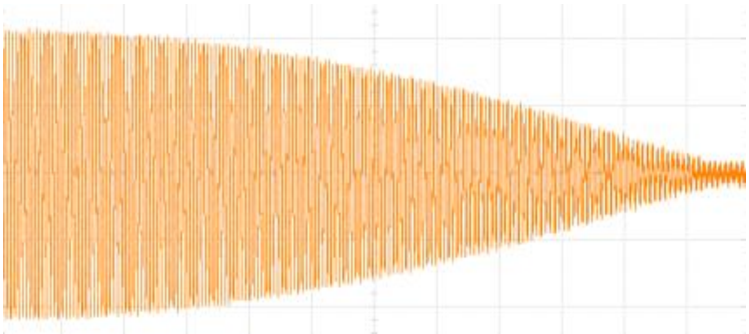


Figure 5-6 Soft-Off Phase Current Wave

5.11 Motor Lock Protection

Motor lock protection circuitry monitors operating state of the motor. When the conditions for motor lock are satisfied, the chip shuts down and waits for 20s to decide whether to restart (depending on software settings).

5.12 Phase Loss Protection

Phase loss protection circuitry monitors operating state of the motor. When the conditions for phase loss are satisfied, the chip shuts down and waits for 20s to decide whether to restart (depending on software settings).

5.13 Current Limiting Protection

The chip supports current limiting protection in sensored SVPWM mode. Cycle-by-cycle current limiting is typically used due to its fast response. The chip turns off the high-side output when it detects the current limiting protection signal, and releases the high-side output until the protection signal is recovered to normal.

5.14 Over-current Protection

When the sampling current exceeds the over-current protection threshold, the chip shuts down and waits for 6s to decide whether to restart (depending on software settings).

5.15 Configurable Maximum Speed Protection

As a means of protection, the maximum running speed can be clamped in sensor-based SVPWM mode at a configurable limit. This is particularly useful as motors may run at a significantly high speed at no-load condition or sensored SVPWM mode. By limiting the running speed, the motor is effectively protected.

6 Revision History

Rev.	Descriptions	Date	Prepared By
V1.0	1. First release, translated from Chinese version 1.0. 2. Added drive current: +0.21A/-0.36A in section 1.3 Features. 3. Added System Clock Frequency in Table 4-2 Global Electrical Characteristics. 4. Added DRV High-level Output Voltage, DRV Low-level Output Voltage, DRV High-level Output Short-circuit Pulse Current and DRV Low-level Output Short-circuit Pulse Current in Table 4-3 IO Electrical Characteristics (DIR/SPEED/FG).	2020/04/27	Eric Deng
V1.1	1. Updated Figure 1-7 Pin Diagram of ET8061L LQFP48; 2. Updated section 1.7 Pin Definitions; 3. Updated Figure 2-1 LQFP48_7X7 Package Dimensions; 4. Added VBS UVLO Threshold Voltage, VBS UVLO Reset Voltage, VCC Reset Voltage VCCUVH and VCC Detection Voltage VCCUVL in Table 4-2 Global Electrical Characteristics; 5. Corrected some grammatical mistakes; 6. Standardized document format.	2023/08/01	Eric Deng
V1.2	1. Modified the repeated "AOP" in Figure 1-3 ET8061L in Sensorless FOC Mode with Single-shunt Current Sampling as "A0M"; 2. Updated section 1.7 Pin Definitions; 3. Updated chapter 2 Package Information; 4. Added section 4.4 PWM/CLOCK Input Frequency, 4.5 6N Pre-driver Electrical Characteristics and 4.6 Speed Control with Analog Voltage; 5. Deleted "Analog voltage for motor speed regulation (ASPEED) pin withstands up to VCC".	2024/01/03	Eric Deng

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