Datasheet

Three-phase BLDC Motor Controller with Built-in MOS

ET8215Q1

Fortior Technology Co., Ltd.

Contents

ET8215Q1 Three-phase BLDC Motor Controller with Built-in MOS

1 System Introduction

1.1 Overview

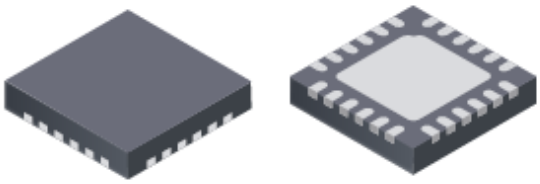
ET8215Q1 is an IC with built-in three-phase MOSFET designed for BLDC motor drive system. Due to a high level of integration, few peripheral components are required. The chip features with low noise and small torque ripple. Motor parameters, startup control parameters and speed regulation mode can be configured via GUI, and are stored in built-in EEPROM. Analog voltage, PWM, I^2C interface or CLOCK mode is optional for motor speed regulation. Moreover, the chip integrates speed indicator, which reads motor speed in real time via FG pin or I^2C interface. Speed control mode, current control mode or voltage-loop control mode is optional. In addition, the chip is secured with a wide range of protection mechanisms, including over-current protection (OCP), under-voltage lockout (UVLO), temperature sensor detect (TSD), motor lock protection (MLP) and phase loss protection. Sleep current of the chip is about 40μA.

1.2 Applications

Fans for car seats.

1.3 Features

- Sensorless FOC mode
- Built-in MOS
- Speed control mode, current control mode or voltage-loop control mode
- Analog voltage, PWM, I^2C interface or CLOCK mode for motor speed regulation
- I^2C interface for motor control and motor states readback
- Rotor initial position detection
- Tailwind and headwind detection
- Soft-On and Soft-Off features
- Drive current: 1A
- Built-in EEPROM
- Configurable multi-segment speed control curve
- Protection against over-current, under-voltage, over-temperature, motor lock and phase loss
- Forward or reverse rotation
- FG and RD output
- AEC-Q100 Certification (Grade 1)



QFN24

1.4 Typical Application Diagram

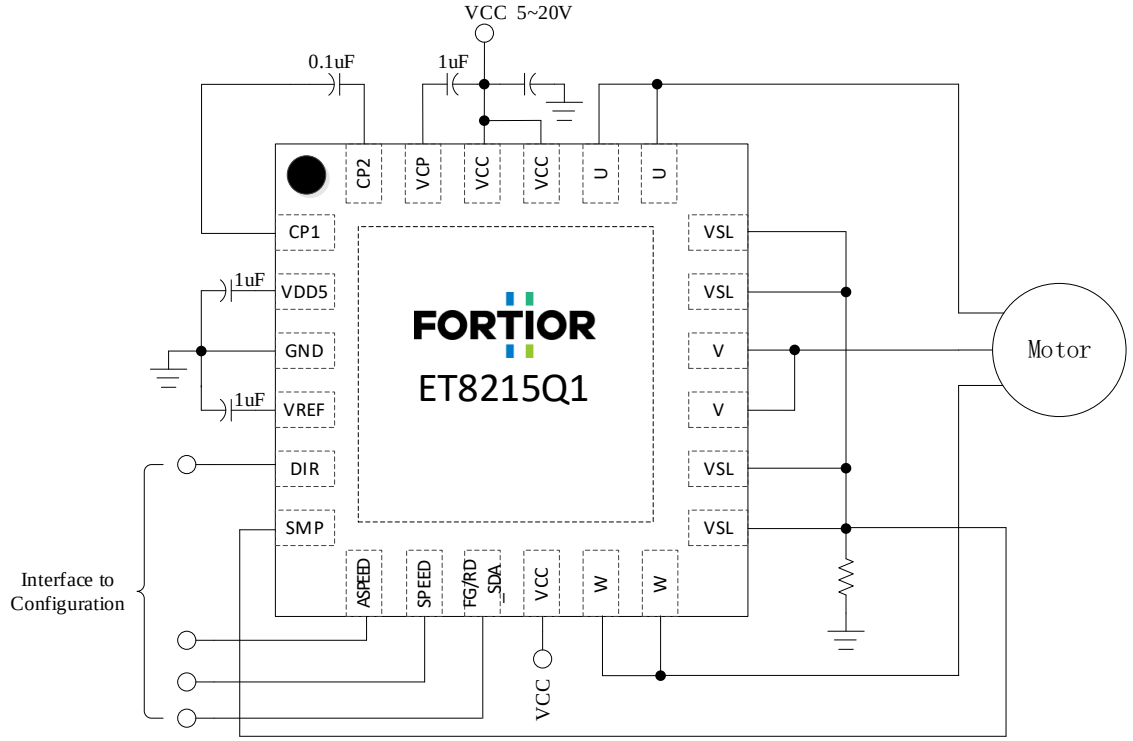


Figure 1-1 Typical Application Diagram of ET8215Q1 (Single-shunt Current Sampling)

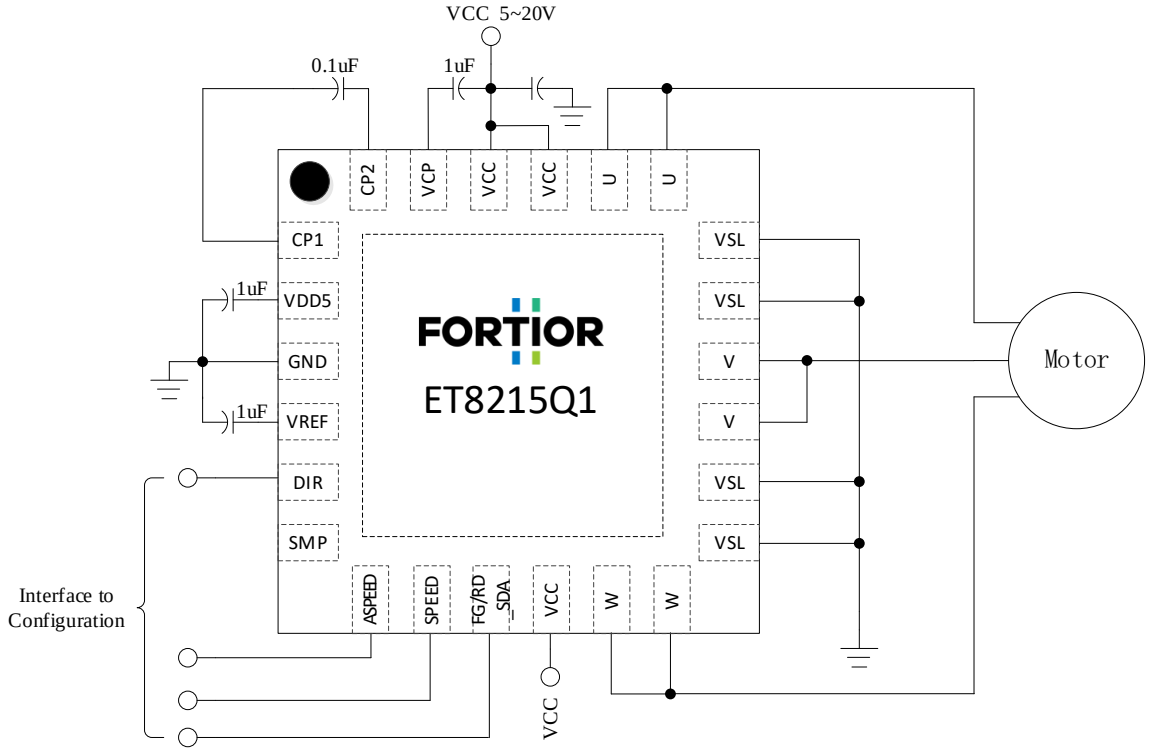


Figure 1-2 Typical Application Diagram of ET8215Q1 (Dual/Triple-shunt Current Sampling)

1.5 Functional Block Diagram

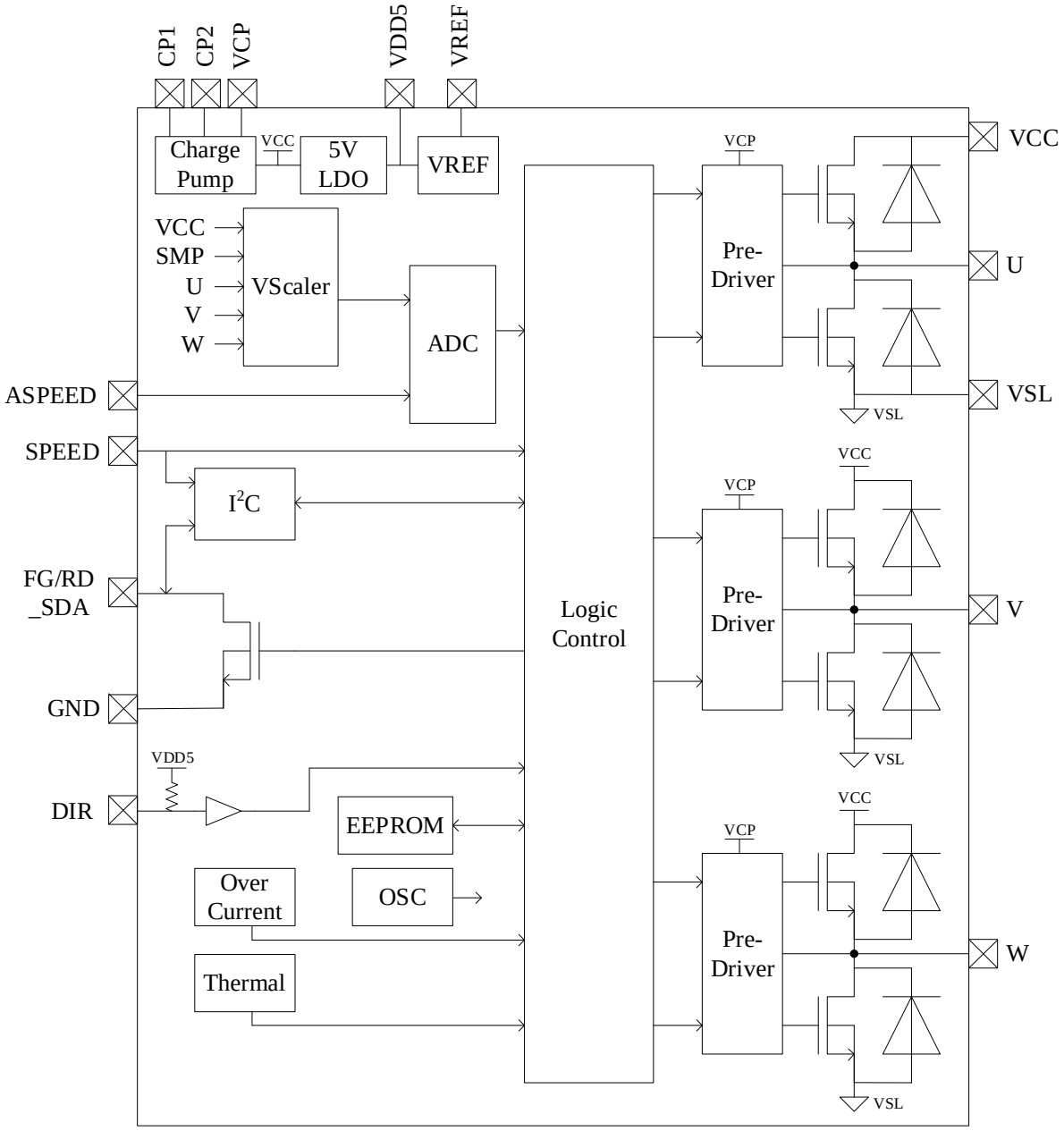


Figure 1-3 Functional Block Diagram of ET8215Q1

1.6 Pinout Diagram

1.6.1 ET8215Q1 QFN24

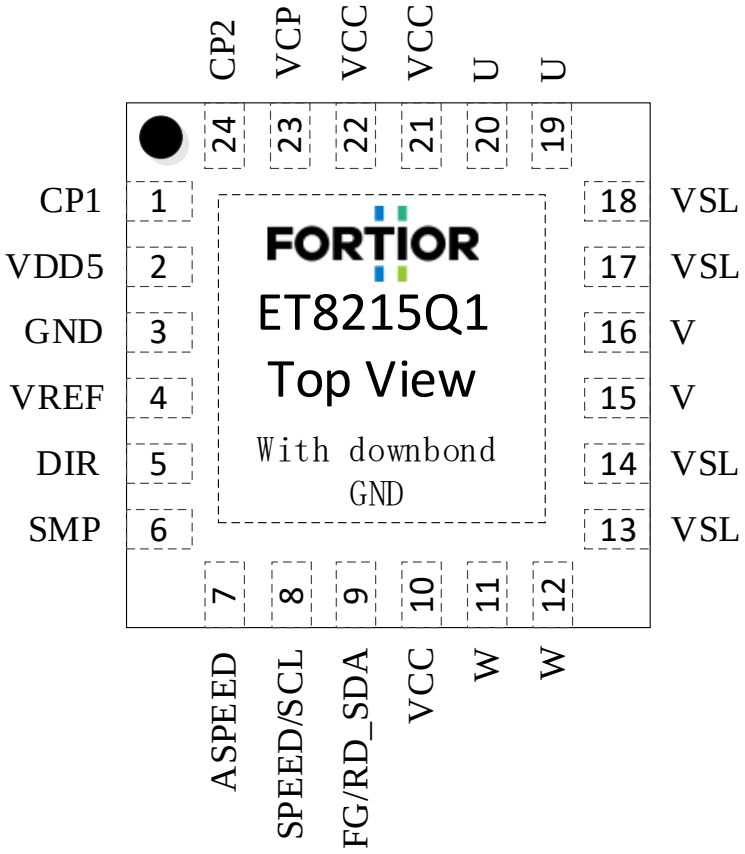


Figure 1-4 Pinout Diagram of ET8215Q1 QFN24

1.7 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analogue Input
- AO = Analogue Output
- P = Power Supply

1.7.1 ET8215Q1 QFN24 Pins

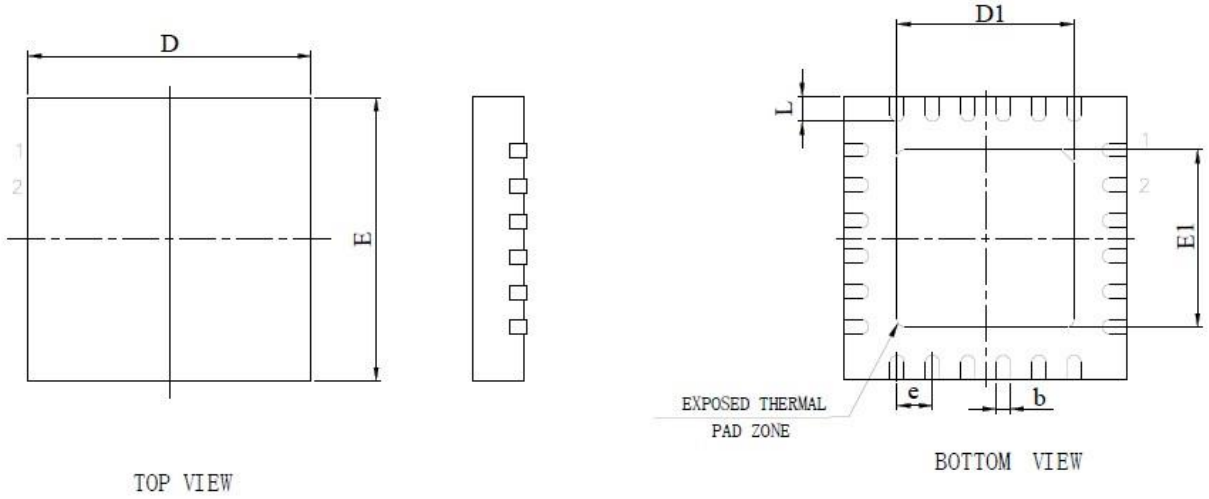
Table 1-1 ET8215Q1 QFN24 Pins

Pin	ET8215Q1 QFN24	IO Type	Description
CP1	1	AO	Charge pump pin, with a 0.1μF capacitor connected between CP2 and CP1 pins
VDD5	2	P	5V LDO output, with an 1μF~4.7μF capacitor connected to ground
GND	3	P	Ground
VREF	4	AI	ADC reference voltage, with an external 1μF capacitor connected to ground
DIR	5	DI	Motor rotation control, with built-in pull-up resistor 0: Reverse output phase sequence: U-->W-->V 1: Forward output phase sequence: U-->V-->W
SMP	6	AI	Bus current sampling input
ASPEED	7	AI	Analog voltage input for motor speed regulation
SPEED/ SCL	8	DI/ DB	Speed control input, PWM speed regulation, CLOCK speed regulation I^2C SCL
FG/RD_ SDA	9	DO/ DB	Speed output signal or motor block indication; Collector open-drain output I^2C SDA; Collector open-drain output
VCC	10	P	Input power supply
W	11	DO	W-phase output
W	12	DO	W-phase output
VSL	13	DO	Low-side ground output
VSL	14	DO	Low-side ground output
V	15	DO	V-phase output
V	16	DO	V-phase output
VSL	17	DO	Low-side ground output
VSL	18	DO	Low-side ground output
U	19	DO	U-phase output
U	20	DO	U-phase output

Pin	ET8215Q1 QFN24	IO Type	Description
VCC	21	P	Input power supply, 5V~20V DC, with an 1μF or above capacitor connected to ground
VCC	22	P	Input power supply
VCP	23	P	Charge pump output, with an 1μF~4.7μF capacitor connected to VCC pin
CP2	24	AO	Charge pump pin, with a 0.1μF capacitor connected between CP2 and CP1 pins

2 Package Information

2.1 QFN24_4X4



QFN24L			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
E	3.9	4	4.1
D	3.9	4	4.1
E1	2.2		2.6
D1	2.2		2.6
L	0.3	0.4	0.5
e		0.5	
b	0.18	0.25	0.3

Figure 2-1 QFN24_4X4 Package Dimensions

3 Ordering Information

Table 3-1 Model Selections

Model	Power Supply (V)	Rdson (High Side + Low Side) (Ω)	Bus Current Average Value (A)	Control Functions						Protection					Operation Temperature T_j (℃)	Lead-free	Package
				Drive Type	Speed Regulation			Forward or Reverse Rotation	Initial Position Detection	OCP	TSD	UVLO	MLP	Phase Loss Protection			
					I²C	PWM/CLOCK	Analog Voltage										
ET8215Q1	5~20	0.25	1	Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	-40~150	√	QFN24 (4x4mm)

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_j		-40	-	150	℃
Storage Temperature T_{stg}		-55	-	150	℃
VCC to VSS Spike Voltage	t < 500mS	-0.3	-	36	V
VCC to VSS Voltage		-0.3	-	22	V
VCC to VSS Voltage	t ≤ 60s	-0.3	-	26	V
VDD5 to VSS Voltage		-0.3	5	6.5	V
FG/U/V/W/CP1 to VSS Voltage		-0.3	-	VCC + 0.3	V
VSL to VSS Voltage		-0.3	-	0.5	V
VCP/CP2 to VSS Voltage		-0.3	-	VCC + 6.0	V
VREF/DIR/SMP/ASPEED/SPEED to VSS Voltage		-0.3	-	VDD5 + 0.3	V

Note: Stress values greater than the "Absolute Maximum Ratings" listed in Table 4-1 Absolute Maximum Ratings may cause irremediable damages to the device. These are stress ratings only, and it is not recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

4.2 Global Electrical Characteristics

Table 4-2 Global Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage		5	-	20	V
VDD5 Operating Voltage	I = 0mA~10mA	4.8	5	5.2	V
VREF		4.3	4.5	4.7	V
VCC Operating Current I_{VCC}	T_A = 25℃	-	-	1	A
	T_A = 125℃	-	-	0.8	A
VCC Sleep-mode Current $I_{VCC\text{-}sleep}$		-	36	-	μA
Rdson (High-side + Low-side)		-	0.22	0.4	Ω

4.3 Protection Electrical Characteristics

Table 4-3 Protection Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC UVLO Voltage V_{UVLO}		3.2	3.5	3.8	V
VCC UVLO Recover Hysteresis Voltage $V_{UVLO\text{-}HYS}$		-	0.5	-	V
I_{ocp} Over-current Threshold		1.8	2	2.2	A
T_{TSD} Temperature Sensor Detect		-	165	-	℃
T_{TSD_HYS} Temperature Hysteresis		-	15	20	℃

4.4 IO Electrical Characteristics (DIR/SPEED/FG)

Table 4-4 IO Electrical Characteristics (DIR/SPEED/FG)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage V_{IH}		2.5	-	VDD5	V
Low-level Input Voltage V_{IL}		0	-	0.6	V
SPEED/DIR/ASPEED Pull-up Resistor	SPEED pin in PWM/CLOCK	-	33	-	kΩ
SPEED Pull-down Resistor	speed regulation mode	-	21	-	kΩ

4.5 PWM/CLOCK Input Frequency Range

Table 4-5 PWM/CLOCK Input Frequency Range

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWM Input Frequency Range		20	-	100k	Hz
CLOCK Input Frequency Range		20	-	1400	Hz

4.6 ASPEED Electrical Characteristics

Table 4-6 ASPEED Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ASPEED Input Voltage Range		0	-	VREF	V

4.7 Thermal Characteristics

Table 4-7 QFN24 Thermal Characteristics

Parameter	Test Conditions	Value	Unit
θ_{JA} Junction-to-ambient Thermal Resistance[1]	JEDEC standard, 2S2P PCB	50	°C/W
θ_{JC} Junction-to-case Thermal Resistance[1]	JEDEC standard, 2S2P PCB	25	°C/W

Note:

[1] Test results may vary depending on the actual conditions.

5 Function Description

5.1 VREF

VREF is applied to internal digital logic and analog circuits only, and cannot be used for external circuits. A capacitor of 1μF or above shall be connected at VREF pin to stabilize the power supply.

5.2 DIR

Forward or reverse direction control (DIR) pin is used to reverse motor rotation by changing DIR level. Pull-ups make the pin state as "High" by default.

5.3 SMP

SMP pin is used as the input of bus current sampling in single-shunt current sampling mode.

5.4 ASPEED

Analog voltage for motor speed regulation (ASPEED) pin withstands up to VCC. When this feature is enabled, analog voltage is input to control motor speed.

5.5 SPEED

Speed control (SPEED) pin is used to input duty cycle for speed regulation depending on the settings. In addition, SPEED pin serves as the clock line (SCL) for I^2C communication.

5.6 FG/RD_SDA

Speed detection and fault indication (FG/RD_SDA) pin is an open-drain output. When this pin is set to FG, it outputs speed feedback signal to indicate rotation speed of the motor, and when it is set to RD, it outputs high-level signal to indicate the fault state. In addition, FG/RD_SDA pin serves as the data line (SDA) for I^2C communication.

5.7 VSL

In single-shunt current sampling mode, this pin is connected to ground with the sampling resistor. In dual/triple-shunt current sampling mode, this pin is short to ground. VSL to VSS voltage cannot be over 0.5V.

5.8 Speed Regulation

5.8.1 Speed Regulation Mode

The chip supports four types of speed control input interface: PWM, analog voltage, I^2C and CLOCK, and only one of them can be chosen at a time. If analog voltage is selected, voltage value input to ASPEED pin controls the speed; if PWM or CLOCK is selected, duty cycle of PWM or CLOCK signal input to SPEED pin controls the speed; and if I^2C is selected, SPEED pin serves as the clock line (SCL) and FG/RD_SDA pin as the data line (SDA).

5.8.2 Speed Regulation Curve

The control waveform is presented as below, where x-coordinate refers to duty cycle of the PWM input pin (In I^2C control and analog control modes, the input is converted to the corresponding PWM duty cycle); and y-coordinate refers to the output duty cycle, which represents different physical quantities in different control modes.

The y-coordinate represents Duty in voltage-loop control mode. The multi-segment speed control curve is obtained by setting five output duty cycle reference points. The start point is determined by X_ON, and the maximum duty cycle PWM_X98 can be set as 98% or 100%. The three inflection points of speed regulation curve are fixed at 25%, 50% and 75%, and the corresponding output reference Y_ON, Y_25, Y_50, Y_75 and Y_MAX are configurable.

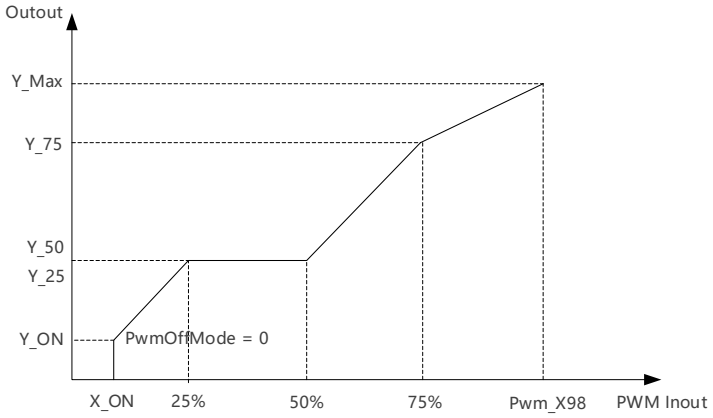


Figure 5-1 Multi Segment Output Curve in Voltage-loop Control Mode (PwmOffMode = 0)

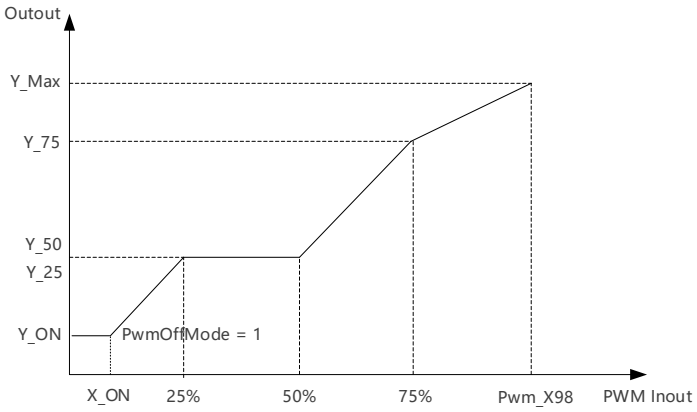


Figure 5-2 Multi Segment Output Curve in Voltage-loop Control Mode (PwmOffMode = 1)

When speed-loop/current-loop control mode is selected, y-coordinate represents motor speed/current. In this case, only Y_ON and Y_MAX are configurable, and the output of other points between them increases linearly as the input varies.

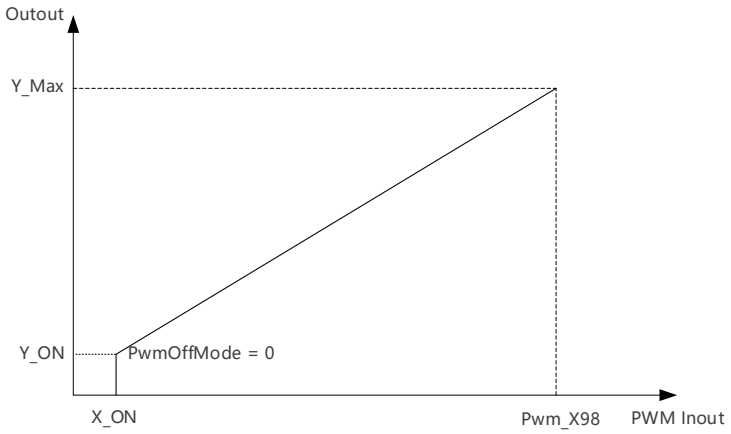


Figure 5-3 Output Curve in Speed/Current-loop Control Mode (PwmOffMode = 0)

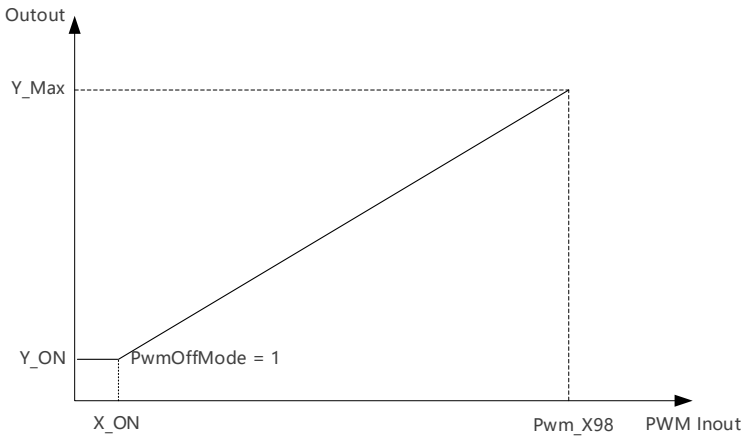


Figure 5-4 Output Curve in Speed/Current-loop Control Mode (PwmOffMode = 1)

5.9 Sleep Mode

The chip enters Sleep mode when the motor stays in stop state for 6 seconds.

Wakeup conditions: In I^2C speed control mode, the chip exits sleep mode after receiving the matched I^2C ID. In PWM or CLOCK speed control mode, if inverted input is disabled, the chip exits sleep mode when a high-level voltage is input to SPEED pin; and if inverted input is enabled, the chip exits sleep mode when a low-level voltage is input to SPEED pin. In analog voltage control mode, the chip exits sleep mode when the voltage of ASPEED pin is greater than 1.5V or when a high-level voltage is input to SPEED pin.

5.10 Soft-On and Soft-Off

Soft-On feature gradually increases the current during start-up process, and Soft-Off feature gradually decreases the current during shut-down process. The two features protect the motor from abrupt startup or shutdown and reduce noise during operation.

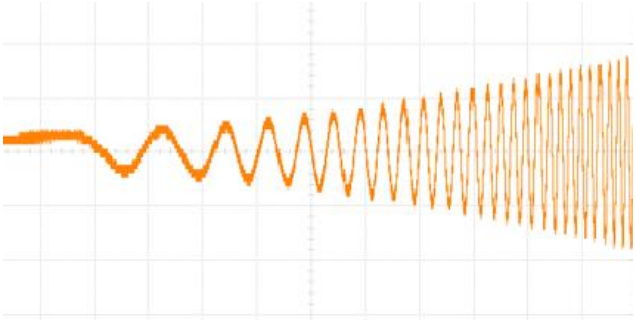


Figure 5-5 Soft-On Phase Current Wave

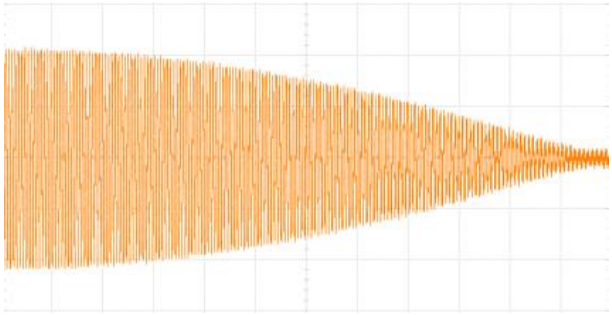


Figure 5-6 Soft-Off Phase Current Wave

5.11 Motor Lock Protection

Motor lock protection circuitry monitors operating state of the motor. When the conditions for motor lock are satisfied, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.12 Phase Loss Protection

Phase loss protection circuitry monitors operating state of the motor. When the conditions for phase loss are satisfied, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.13 Over-current Protection

When the sampling current exceeds the over-current protection threshold, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.14 Frequency Multiplication and Division of FG

Configuring FG/RD to FG outputs FG signal, that is, FG/RD_SDA pin is selected to output FG signal.

The output frequency of FG signal is determined by FGDIV (frequency division coefficient) and FGMUL (frequency multiplication coefficient). FGMUL can be set as 1, 2, 3 and 4, while FGDIV as 1, 1/3, 1/4 and 1/5. k (coefficient of output frequency) = FGMUL*FGDIV.

Table 5-1 FG Configurations

Coefficient of Output Frequency (k)		FGMUL			
		1	**2**	**3**	**4**
FGDIV	**1**	1	2	3	4
	1/3	1/3	2/3	3/3	4/3
	1/4	1/4	2/4	3/4	4/4
	1/5	1/5	2/5	3/5	4/5

The number of FG signals in one mechanical cycle is equal to pp*k (pp refers to pole-pair number of the motor).

Example: For a 4-pole-pair motor, if FGMUL is set as 3 and FGDIV as 1/4, that is, k = 3/4, three FG signals are displayed in one mechanical cycle (4 * 3/4).

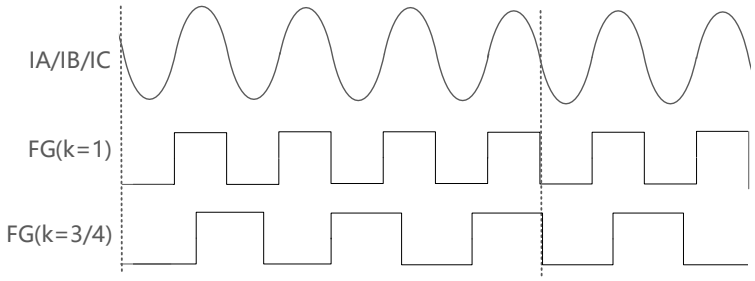


Figure 5-7 FG Output Waveforms When k = 1 and k = 3/4

5.15 CLOCK Speed Regulation Mode

In this mode, SPEED pin serves as the input of reference PWM frequency, and motor speed changes with reference PWM frequency. FGMUL and FGDIV are used to set the factor between motor speed and reference PWM frequency: Motor Speed = (reference PWM frequency*60/pp)/(FGMUL*FGDIV).

Example: For a 5-pole-pair motor, if FGDIV is set as 1/3 and FGMUL as 2 (i.e., k = 2/3), and the reference PWM frequency is 100Hz, then motor speed = (100Hz*60/5) / (2/3) = 1800rpm.

6 Revision History

Rev.	Descriptions	Date	Prepared By
V1.1	First release, translated from Chinese version 1.1.	2023/05/19	Eric Deng
V1.2	1. Added definition of DB to Pin Definitions； 2. Modified FG/SDA as FG/RD_SDA, ASPD as ASPEED and SPD as SPEED in 1.4 Typical Application Diagram; 3. Modified FG/SDA as FG/RD_SDA in Figure 1-3 Functional Block Diagram of ET8215Q1; 4. Modified FG/SDA as FG/RD_SDA in Figure 1-4 Pinout Diagram of ET8215Q1 QFN24; 5. Updated descriptions on SCL pin (No. 8), FG/SDA pin (No.9) and VCC pin (No. 21) in 1.7.1 ET8215Q1 QFN24 Pins; 6. Updated 2 Package Information; 7. Modified FG as FG/RD_SDA in 5.6 FG and 5.8.1 Speed Regulation Mode; 8. Modified FG/RD pin as FG/RD_SDA pin in 5.14 Frequency Multiplication and Division of FG; 9. Proofread 1 System Introduction; 10. Standardized document format.	2023/06/14	Eric Deng
V1.3	Added “AEC-Q100 Certificate (Grade 1)” in section 1.3 Features	2023/06/14	Kelly Li
V1.4	Added the parameter “VCC to VSS voltage ($t \leq 60s$)” in Table 4-1 Absolute Maximum Ratings	2023/06/27	Kelly Li
V1.5	1. Updated Figure 2-1 QFN24_4X4 Package Dimensions; 2. Modified I2C as I^2C.	2023/08/16	Eric Deng

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