Datasheet

Three-phase BLDC Motor Controller with Built-in MOSFET

FT8215Q

Fortior Technology (Shenzhen) Co., Ltd

Contents

FT8215Q Three-phase BLDC Motor Controller with Built-in MOSFET

1 System Introduction

1.1 Overview

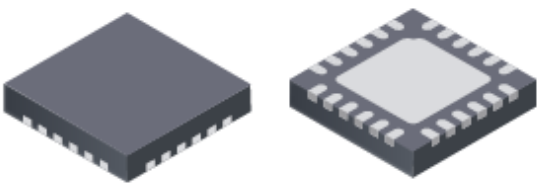
FT8215Q is an IC with built-in three-phase MOSFET designed for BLDC motor drive system. Due to a high level of integration, few peripheral components are required. The chip features with low noise and small torque ripple. Motor parameters, startup control parameters and speed regulation mode can be configured via GUI, and are stored in built-in EEPROM. Analog voltage, PWM, I2C interface or CLOCK mode is optional for motor speed regulation. Moreover, the chip integrates speed indicator, which reads motor speed in real time via FG pin or I2C interface. Speed control mode, current-loop control mode or voltage-loop control mode is optional. In addition, the chip is secured with a wide range of protection features, including over-current protection (OCP), under-voltage lockout (UVLO), temperature sensor detect (TSD), motor lock protection (MLP) and phase loss protection. Sleep current of the chip is about 40μA.

1.2 Applications

Floor fans, cooling fans, etc.

1.3 Features

- Sensorless FOC mode
- Built-in MOS
- Speed control mode, current-loop control mode or voltage-loop control mode
- Analog voltage, PWM, I2C interface or CLOCK mode for motor speed regulation
- Real-time information interactions by I2C for motor control and motor states readback
- Support initial position detection
- Tailwind and headwind detection
- Soft-on and soft-off features
- Drive current: 2A (average value)
- Built-in EEPROM
- Configurable multi-segment output curve
- Protection against over-current, under-voltage, over-temperature, motor lock and phase loss
- Forward or reverse rotation direction selectable
- FG and RD output



QFN24

1.4 Typical Application Diagram

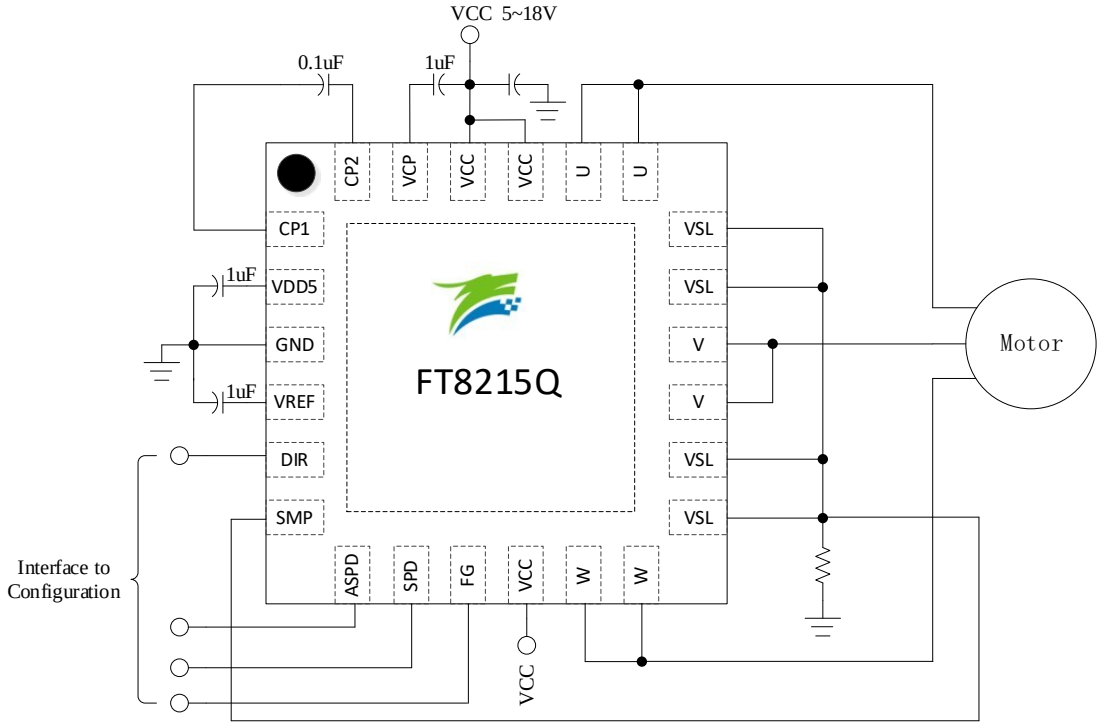


Figure 1-1 Typical Application Diagram of FT8215Q (Single-shunt Current Sampling)

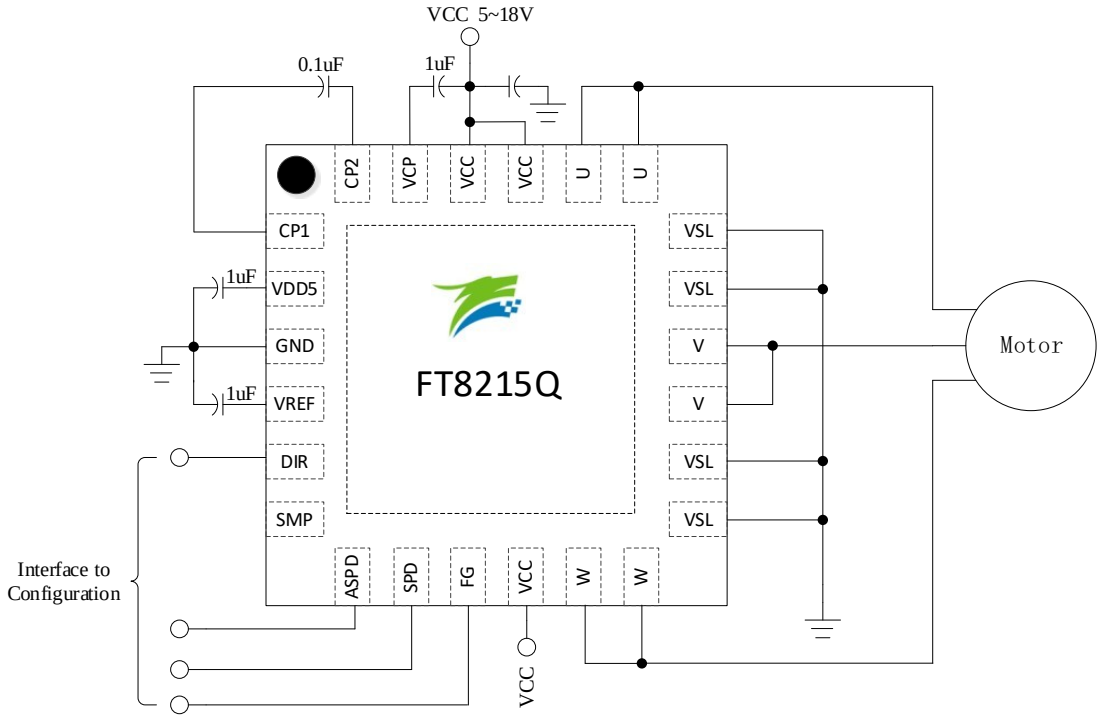


Figure 1-2 Typical Application Diagram of FT8215Q (Dual/Triple-shunt Current Sampling)

1.5 Functional Block Diagram

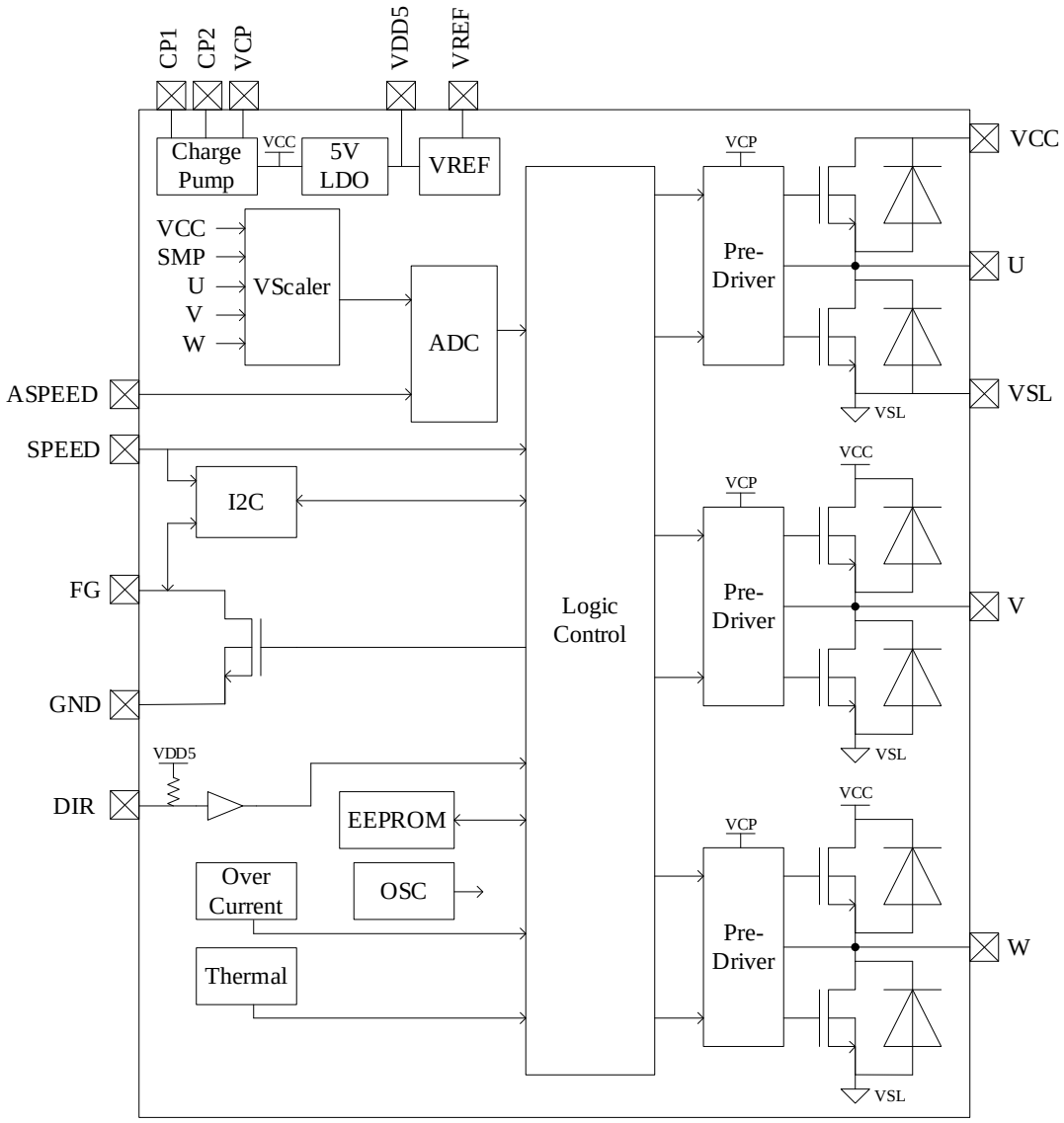


Figure 1-3 Functional Block Diagram of FT8215Q

1.6 Pinout Diagram

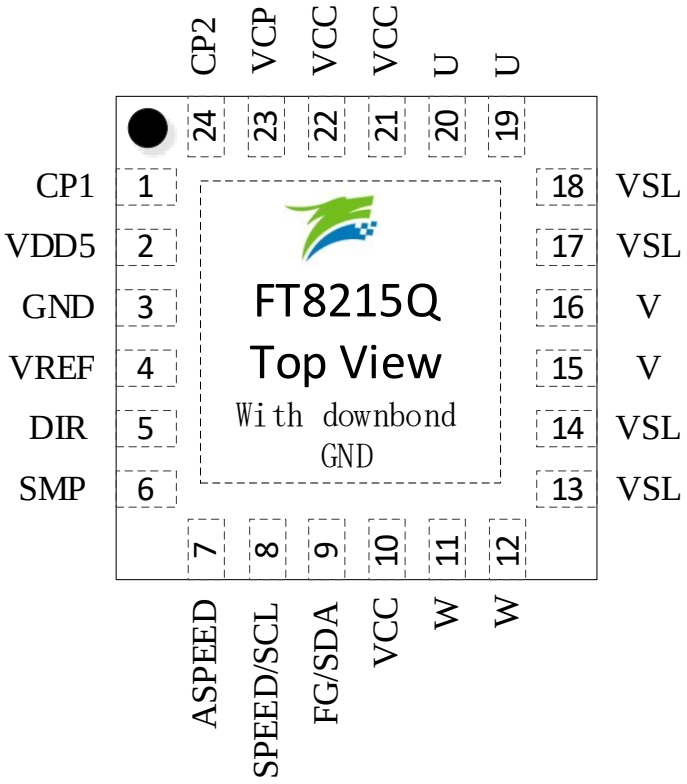


Figure 1-4 Pinout Diagram of FT8215Q QFN24

1.7 Pin Definitions

Table 1-1 FT8215Q QFN24 Pins

Pin	FT8215Q QFN24	IO Type	Description
CP1	1	AO	Charge pump pin, with a 0.1μF capacitor connected between CP2 and CP1 pins
VDD5	2	P	5V LDO output, with an 1μF~4.7μF capacitor connected to ground
GND	3	P	Ground
VREF	4	AI	ADC reference voltage, with an external 1μF capacitor connected to ground
DIR	5	DI	Motor rotation control, with built-in pull-up resistor 0: Reverse output phase sequence: U-->W-->V 1: Forward output phase sequence: U-->V-->W
SMP	6	AI	Bus current sampling input
ASPEED	7	AI	Analog voltage input for motor speed regulation
SPEED/ SCL	8	DI/ DB	Speed control input, PWM speed regulation, CLOCK speed regulation I2C SCL
FG/ SDA	9	DO/ DB	Speed output signal or motor block indication; Collector open-drain output I2C SDA
VCC	10	P	Input power supply
W	11	DO	W-phase output
W	12	DO	W-phase output
VSL	13	DO	Low-side ground output
VSL	14	DO	Low-side ground output
V	15	DO	V-phase output
V	16	DO	V-phase output
VSL	17	DO	Low-side ground output
VSL	18	DO	Low-side ground output
U	19	DO	U-phase output
U	20	DO	U-phase output
VCC	21	P	Input power supply, 5V~18V DC, with a capacitor of 1μF or above connected to ground
VCC	22	P	Input power supply
VCP	23	P	Charge pump output, with a 1μF~4.7μF capacitor connected to VCC pin
CP2	24	AO	Charge pump pin, with a 0.1μF capacitor connected between CP2 and CP1 pins

Notes:

- DI = Digital Input
- DO = Digital Output
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

2 Package Information

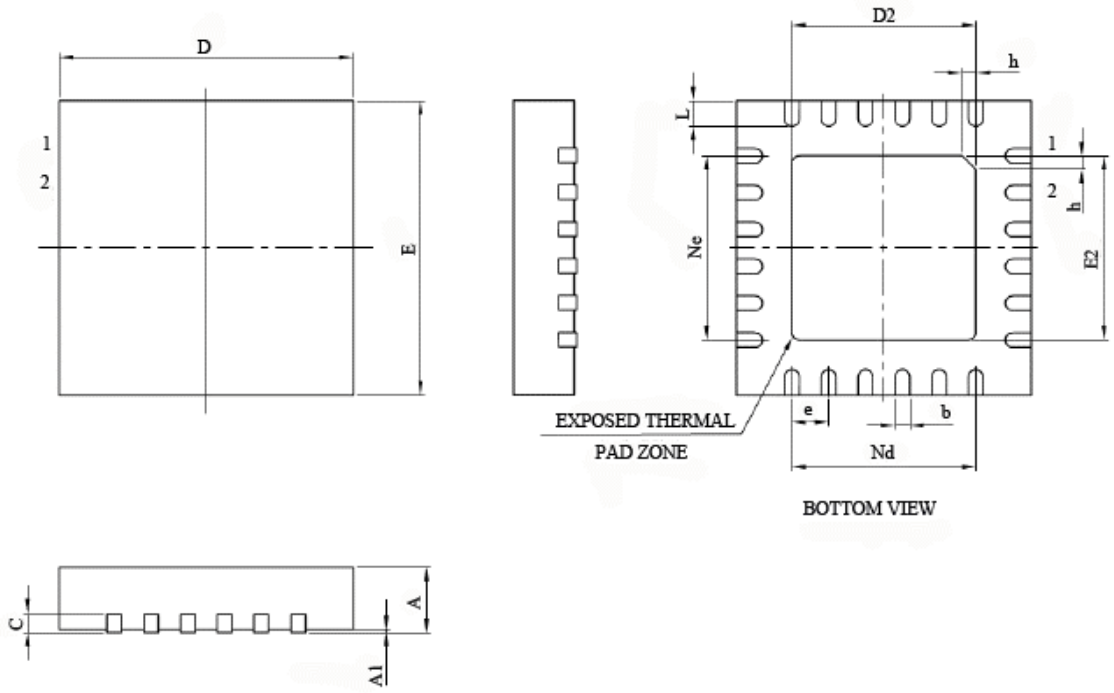


Figure 2-1 QFN24_4X4 Package Drawings

Table 2-1 QFN24_4X4 Package Size Dimensions

Symbol	Dimensions In Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.35	2.50	2.65
L	0.35	0.40	0.45
h	0.30	0.35	0.40
N	Pin Number = 24		

3 Ordering Information

Table 3-1 Package Type Information

Type	Package	Power Supply (V)	Rdson (High-side + Low-side) (Ω)	Bus Current Average Value (A)	Control Functions						Protection					Operation Temperature T_j (°C)	Lead-free
					Driver Type	Speed Regulation			Forward and Reverse Rotation	Initial Position Detection	OCP	TSD	UVLO	MLP	Phase Loss Protection		
						I2C	PWM/CLOCK	Analog Voltage									
FT8215Q	QFN24 (4x4mm)	5 ~ 18	0.25	2	Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	–40 ~ 150	√

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_j		–40	—	150	℃
Storage Temperature T_{stg}		–55	—	150	℃
VCC to VSS Voltage		–0.3	—	22	V
VDD5 to VSS Voltage		–0.3	5	6.5	V
FG, U, V, W and CP1 to VSS Voltage		–0.3	—	VCC + 0.3	V
VSL to VSS Voltage		–0.3	—	0.5	V
VCP/CP2 to VSS Voltage		–0.3	—	VCC + 6.0	V
VREF/DIR/SMP/ASPEED/SPEED to VSS Voltage		–0.3	—	VDD5 + 0.3	V

Note: Stress values greater than the "Absolute Maximum Ratings" listed in Table 4-1 may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

4.2 Global Electrical Characteristics

Table 4-2 Global Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage		5	—	18	V
VDD5 Operating Voltage	I = 0 ~ 10mA	4.8	5	5.2	V
VREF		4.3	4.5	4.7	V
VCC Operating Current I_{VCC}	T_A = 25℃ (Average)	—	—	2	A
	T_A = 85℃ (Average)	—	—	1.8	A
VCC Sleep-mode Current $I_{VCC\text{-}sleep}$		—	36	—	μA
Peak Phase Current I_{PHASE}	Sine-wave Peak Current	—	—	3.0	A
Rdson (High-side MOS + Low-side MOS)		—	0.22	0.4	Ω

4.3 Protection Electrical Characteristics

Table 4-3 Protection Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC UVLO Threshold Voltage V_{UVLO}		3.2	3.5	3.8	V
VCC UVLO Hysteresis Voltage $V_{UVLO\text{-}HYS}$		—	0.5	—	V
I_{ocp} Over-current Threshold		3.5	4.0	4.5	A
T_{TSD} Temperature Sensor Detect		—	165	—	℃
T_{TSD_HYS} Temperature Hysteresis		—	15	20	℃

4.4 IO Electrical Characteristics (DIR/SPEED/FG)

Table 4-4 IO Electrical Characteristics (DIR/SPEED/FG)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage V_{IH}		2.5	—	VDD5	V
Low-level Input Voltage V_{IL}		0	—	0.6	V
SPEED/DIR/ASPEED Pull-up Resistor	SPEED pin in PWM/CLOCK speed regulation mode	—	33	—	kΩ
SPEED Pull-down Resistor		—	21	—	kΩ

4.5 PWM/CLOCK Input Frequency Range

Table 4-5 PWM/CLOCK Input Frequency Range

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWM Input Frequency Range		20	—	100k	Hz
CLOCK Input Frequency Range		20	—	1400	Hz

4.6 ASPEED Electrical Characteristics

Table 4-6 ASPEED Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ASPEED Input Voltage Range		0	—	VREF	V

4.7 Package Thermal Characteristics

Table 4-7 QFN24 Package Thermal Characteristics

Parameter	Test Conditions	Value	Unit
θ_{JA} Junction-to-ambient Thermal Resistance[1]	JEDEC standard, 2S2P PCB	50	°C/W
θ_{JC} Junction-to-case Thermal Resistance[1]	JEDEC standard, 2S2P PCB	25	°C/W

Note:

[1] Test results may vary depending on the actual conditions

5 Function Description

5.1 VREF

VREF is applied to internal digital logic and analog circuits only, and cannot be used for external circuits. A capacitor of 1μF or above shall be connected at VREF pin to stabilize the power supply.

5.2 DIR

Forward or reverse direction control (DIR) pin is used to reverse motor rotation by changing DIR level. Pull-ups make the pin state as "High" by default.

5.3 SMP

SMP pin is used as the input of bus current sampling in single-shunt current sampling mode.

5.4 ASPEED

When analog speed regulation is enabled, analog voltage for motor speed regulation (ASPEED) pin is used to input analog voltage for motor speed regulation.

5.5 SPEED

Speed control (SPEED) pin is used to input duty cycle for speed regulation depending on the settings. In addition, SPEED pin serves as the clock line (SCL) for I2C communication.

5.6 FG

Speed detection and fault indication pin is an open-drain output. When this pin is set to FG, it outputs speed feedback signal to indicate rotation speed of the motor, and when it is set to RD, it outputs high-level signal to indicate the fault state. In addition, FG pin serves as the data line (SDA) for I2C communication.

5.7 VSL

In single-shunt current sampling mode, this pin is connected to ground with the sampling resistor. In dual/triple-shunt current sampling mode, this pin is short to ground. VSL to VSS voltage cannot be over 0.5V.

5.8 Speed Regulation

5.8.1 Speed Regulation Mode

The chip supports four types of speed control input interface: PWM, analog voltage, I2C and CLOCK, and only one of them can be chosen at a time. If analog voltage is selected, voltage value input to ASPEED pin controls the speed; if PWM or CLOCK is selected, duty cycle of PWM or CLOCK signal input to SPEED pin controls the speed; and if I2C is selected, SPEED pin serves as the clock line (SCL) and FG pin as the data line (SDA).

5.8.2 Speed Regulation Curve

The control waveform is presented as below, where x-coordinate refers to duty cycle of the PWM input (In

I2C control and analog control modes, the input is converted to the corresponding PWM duty cycle); and y-coordinate refers to the output duty cycle, which represents different physical quantities in different control modes.

The y-coordinate represents Duty in voltage-loop control mode. The multi-segment speed control curve is obtained by setting five output duty cycle reference points. The start point is determined by X_ON, and the maximum duty cycle PWM_X98 can be set as 98% or 100%. The three inflection points of speed regulation curve are fixed at 25%, 50% and 75%, and the corresponding output reference Y_ON, Y_25, Y_50, Y_75 and Y_MAX are configurable.

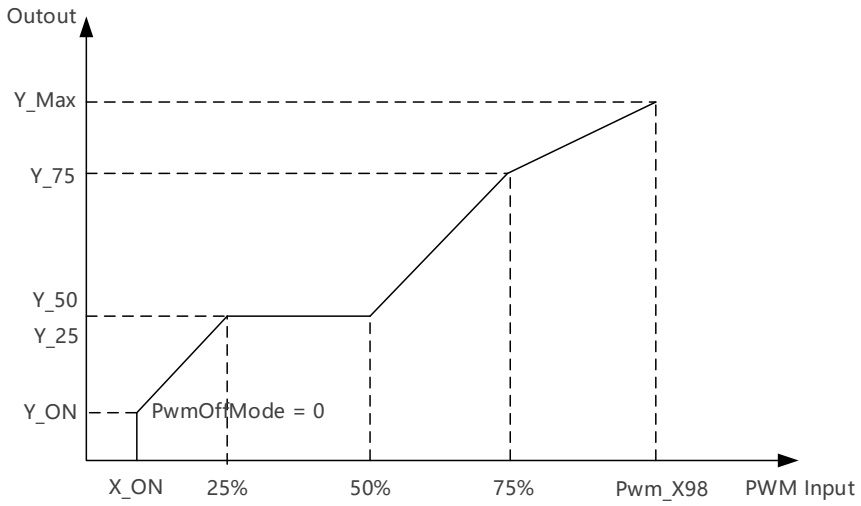


Figure 5-1 Multi-segment Output Curve in Voltage-loop Control Mode (PwmOffMode = 0)

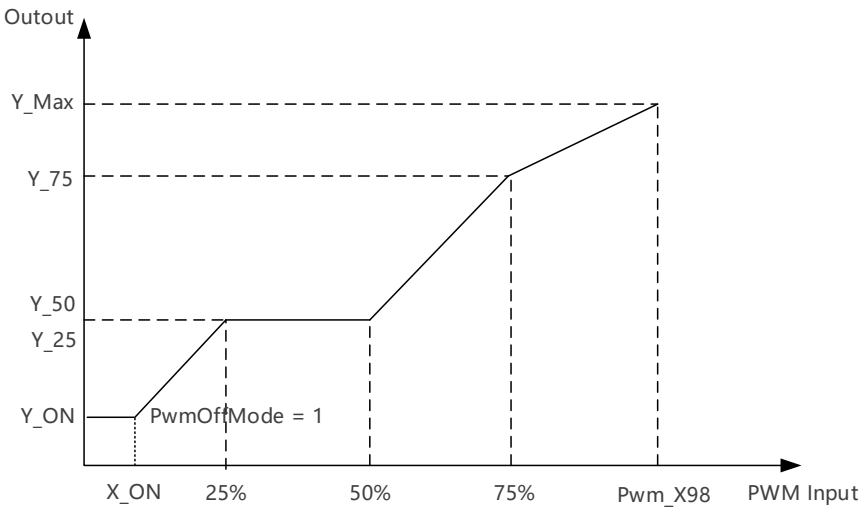


Figure 5-2 Multi-segment Output Curve in Voltage-loop Control Mode (PwmOffMode = 1)

When speed/current-loop control mode is selected, y-coordinate represents motor speed/current. In this case, only Y_ON and Y_MAX are configurable, and the output of other points between them increases linearly as the input varies.

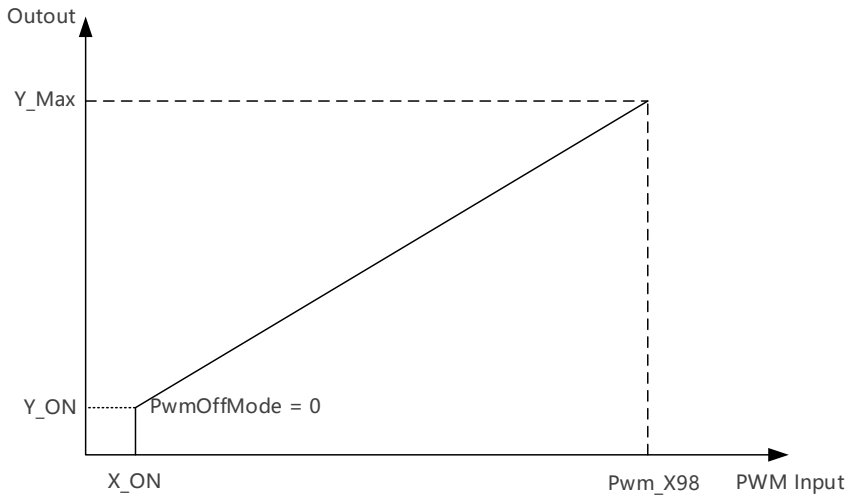


Figure 5-3 Output Curve in Speed/Current-loop Control Mode (PwmOffMode = 0)

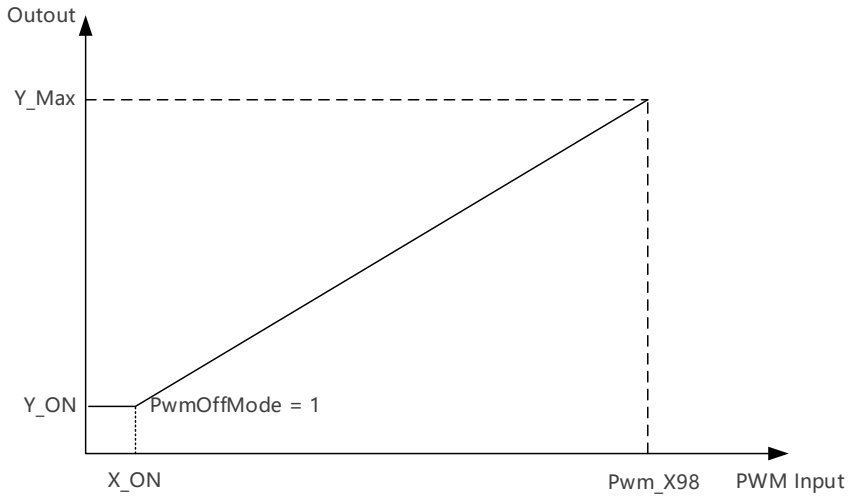


Figure 5-4 Output Curve in Speed/Current-loop Control Mode (PwmOffMode = 1)

5.9 Sleep Mode

The chip enters Sleep mode when the motor stays in stop state for 6 seconds.

Wakeup conditions: In I2C speed control mode, the chip exits sleep mode after receiving the matched I2C ID. In PWM or CLOCK speed control mode, if inverted input is disabled, the chip exits sleep mode when a high-level voltage is input to SPEED pin; and if inverted input is enabled, the chip exits sleep mode when a low-level voltage is input to SPEED pin. In analog voltage control mode, the chip exits sleep mode when the voltage of ASPEED pin is greater than 1.5V or when a high-level voltage is input to SPEED pin.

5.10 Soft-on and Soft-off

Soft-on feature gradually increases the current during start-up process, and Soft-off feature gradually decreases the current during shut-down process. The two features protect the motor from abrupt startup or shutdown and reduce noise during operation.

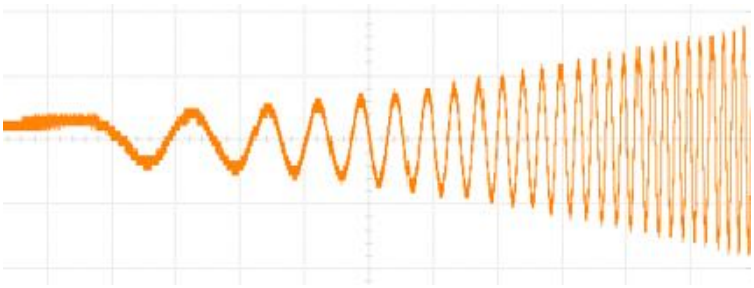


Figure 5-5 Soft-on Phase Current Wave

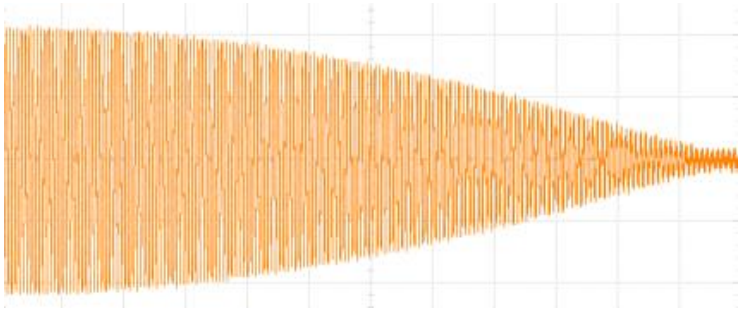


Figure 5-6 Soft-off Phase Current Wave

5.11 Motor Lock Protection

Motor lock protection circuitry monitors operating state of the motor. When the conditions for motor lock are satisfied, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.12 Phase Loss Protection

Phase loss protection circuitry monitors operating state of the motor. When the conditions for phase loss are satisfied, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.13 Over-current Protection

When the sampling current exceeds the over-current protection threshold, the chip shuts down and waits for 4s to decide whether to restart (depending on software settings).

5.14 Frequency Multiplication and Division of FG

Configuring FG/RD to FG outputs FG signal, that is, FG/RD pin is selected to output FG signal. The output frequency of FG signal is determined by FGDIV (frequency division coefficient) and FGMUL (frequency multiplication coefficient). FGMUL can be set as 1, 2, 3 and 4, while FGDIV as 1, 1/3, 1/4 and 1/5. k (coefficient of output frequency) = FGMUL*FGDIV.

Table 5-1 FG Configurations

Coefficient of Output Frequency (k)		FGMUL			
		1	2	3	4
FGDIV	1	1	2	3	4
	1/3	1/3	2/3	3/3	4/3
	1/4	1/4	2/4	3/4	4/4
	1/5	1/5	2/5	3/5	4/5

The number of FG signals in one mechanical cycle is equal to pp*k (pp refers to pole-pair number of the motor).

Example: For a 4-pole-pair motor, if FGMUL is set as 3 and FGDIV as 1/4, that is, k = 3/4, three FG signals are displayed in one mechanical cycle (4 * 3/4).

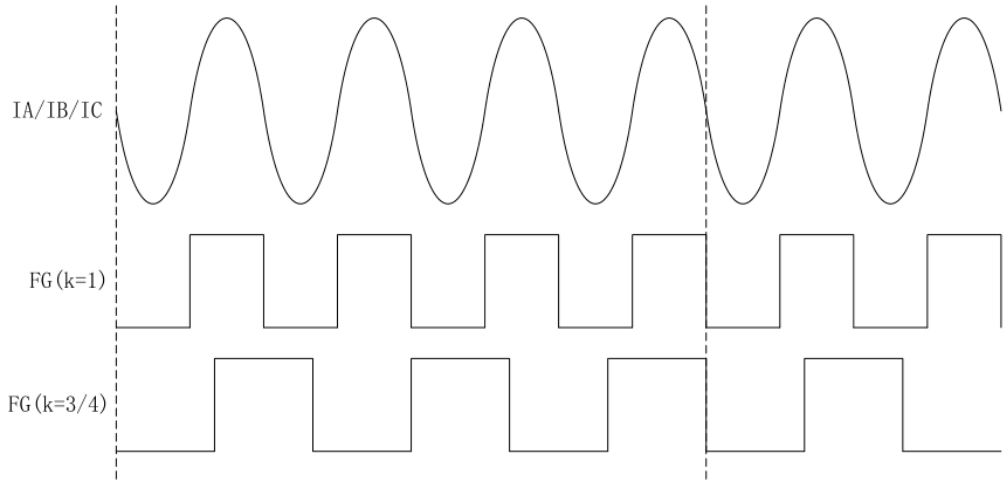


Figure 5-7 FG Output Waveforms When k = 1 and k = 3/4

5.15 CLOCK Speed Regulation Mode

In this mode, SPEED pin serves as the input of reference PWM frequency, and motor speed changes with reference PWM frequency. FGMUL and FGDIV are used to set the factor between motor speed and reference

PWM frequency: Motor Speed = (reference PWM frequency*60/pp)/(FGMUL*FGDIV).

Example: For a 5-pole-pair motor, if FGDIV is set as 1/3 and FGMUL as 2 (i.e., k = 2/3), and the reference PWM frequency is 100Hz, then motor speed = (100Hz*60/5) / (2/3) = 1800rpm. In this case, the output frequency of FG signal is determined by FGDIV and FGMUL.

6 Revision History

Rev.	Descriptions	Date	Prepared By
V1.0	Initial version	2021/01/11	Bruce Long
V1.1	1. Added Chapter 4 Electrical Characteristics. 2. Added Chapter 5 Function Description.	2021/12/23	Bruce Long
V1.2	1. Added more information in Chapter 5. 2. Changed document format.	2021/12/28	Shawn Liang
V1.3	Standardized document format.	2022/04/19	Black Hu
V1.4	Minor content and format change.	2022/06/09	Michelle Xie
V1.5	1. Corrected the model number from FT8132Q to FT8215Q in Table 1-1 FT8215Q QFN24 Pin List; 2. Corrected minimum value of PWM Input Frequency Range from 100 Hz to 20Hz in Table 4-5 PWM/CLOCK Input Frequency Range; 3. Added "If there are any differences between the Chinese and the English contents, please take the Chinese version as the standard." in Copyright Notice; 4. Standardized document format.	2023/03/29	Eric Deng
V1.5Beta	1. Corrected maximum and minimum values of VCC Operating Voltage from 6V and 28V to 5V and 18V respectively in Table 4-2 Global Electrical Characteristics; 2. Added descriptions on SCL and SDA pins in Table 1-1 FT8215Q QFN24 Pins; 3. Modified waiting time for the chip to reset from 6s to 4s in sections 5.11 Motor Lock Protection, 5.12 Phase Loss Protection and 5.13 Over-current Protection; 4. Proofread the entire document and corrected wrong words.	2023/07/07	Eric Deng

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