Datasheet

Three-phase BLDC Motor Controller with Built-in Pre-driver

FT8132

Fortior Technology (Shenzhen) Co., Ltd

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FT8132 Three-phase BLDC Motor Controller with Built-in Pre-driver

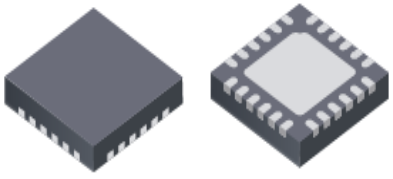
1 System Introduction

1.1 Overview

FT8132 is an IC with built-in three-phase pre-driver designed for BLDC motor drive system. Due to a high level of integration, the chip has few peripheral components and is featured with low noise and small torque ripple. Motor parameters, startup control parameters and speed regulation mode can be configured via GUI, and are stored in built-in EEPROM. Analog voltage, PWM, I^2C interface or CLOCK mode is available for motor speed regulation. Moreover, the chip integrates speed indicator to read motor speed in real time via FG pin or I^2C interface. Speed-loop, current-loop, power-loop or voltage-loop control mode is optional. In addition, the chip is secured with various protection features, including over-current protection (OCP), under-voltage lockout (UVLO), over-voltage lockout (OVLO), motor lock protection (MLP), phase loss protection, abnormal Hall input detection (HALLERR) protection, etc. Sleep current of the chip is about 60μA.

1.2 Applications

Pedestal fans, cooling fans, ceiling fans, robot vacuum cleaners, vacuum cleaners, etc.



QFN24

1.3 Features

- Sensorless FOC
- Hall-based FOC (Hall-IC/Hall-Sensor)
- Hall-based SVPWM (Hall-IC/Hall-Sensor)
- 3P3N pre-driver with configurable deadtime
- Speed-loop, current-loop, power-loop or voltage-loop control mode
- Analog voltage, PWM, I^2C interface or CLOCK mode for motor speed regulation
- Real-time information interactions by I^2C for motor control and motor states readback
- Rotor initial position detection
- Tailwind and headwind detection
- Soft-on and soft-off features
- Built-in EEPROM
- Configurable multi-segment output curve
- Configurable multi-segment output curve
- Support protection features, including OCP, UVLO, OVLO, MLP, phase loss protection, abnormal Hall input detection (HALLERR) protection, etc.
- Forward or reverse rotation selectable
- FG and RD output

SSOP24

1.4 Typical Application Diagram

1.4.1 Sensorless FOC with Dual-shunt Current Sampling

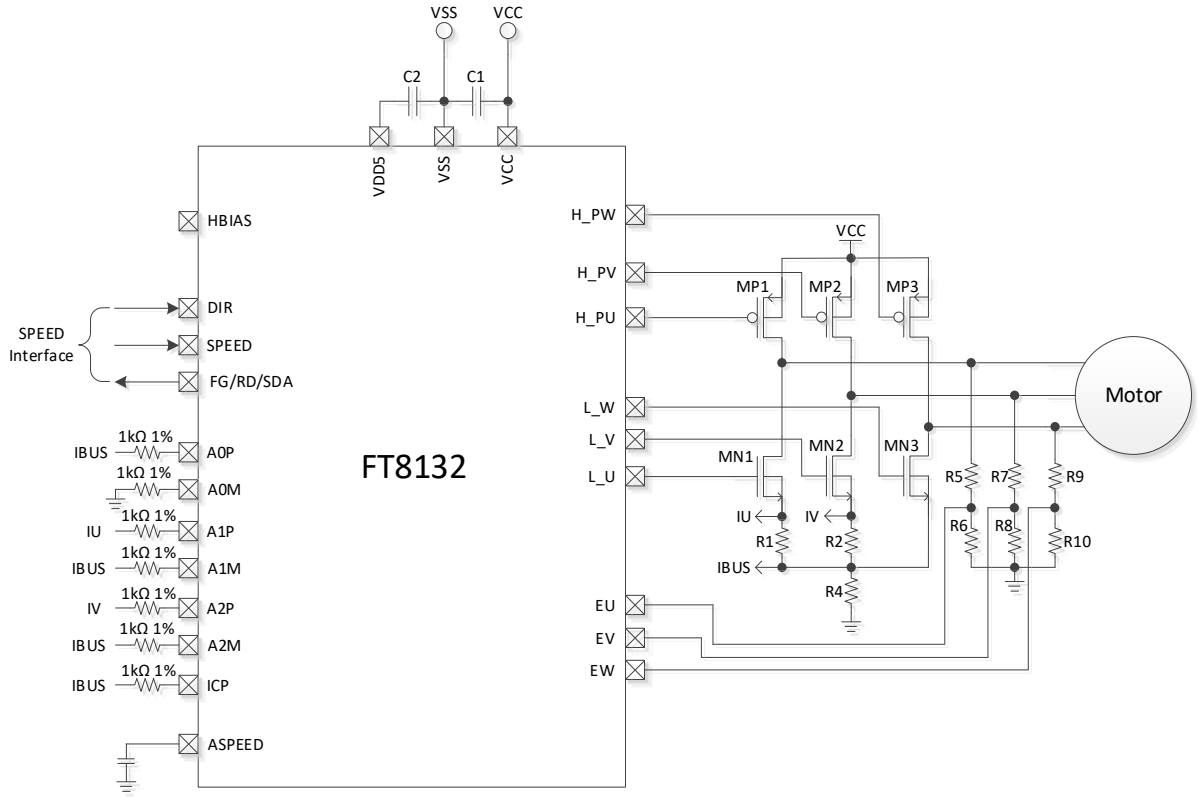


Figure 1-1 Sensorless FOC with Dual-shunt Current Sampling

1.4.2 Hall-Sensor with Single-shunt Current Sampling

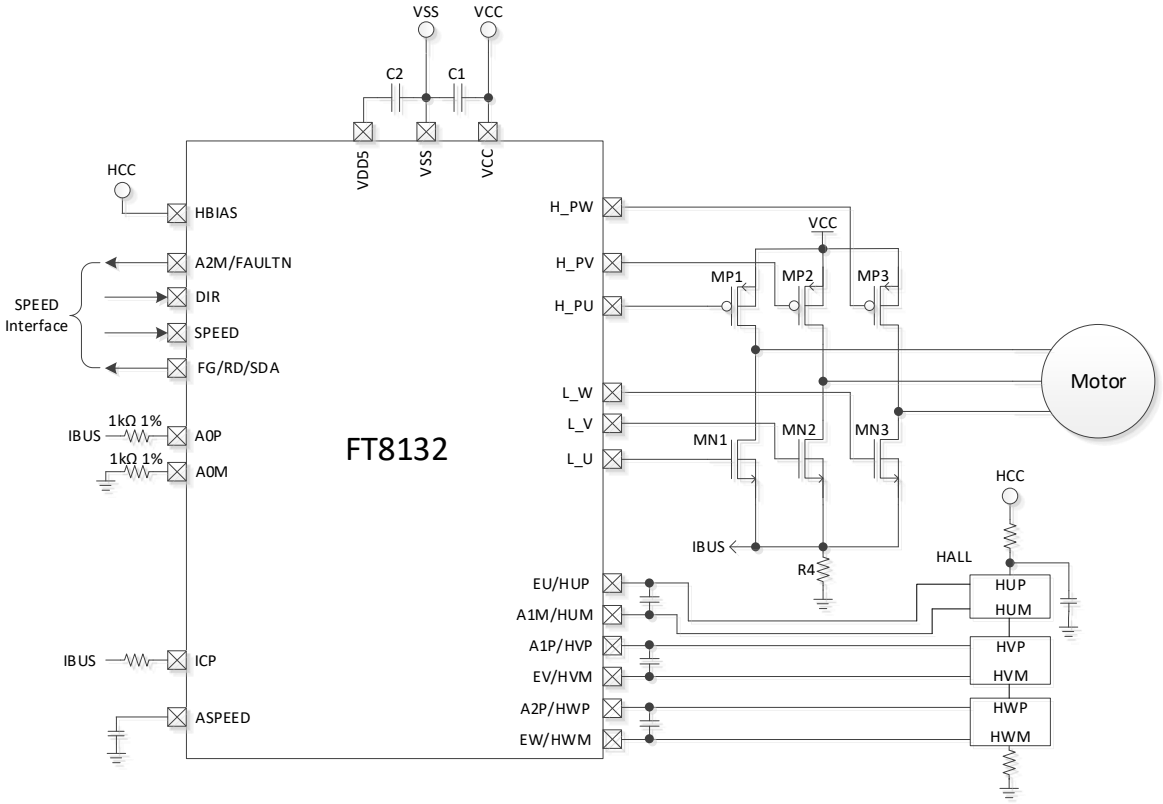


Figure 1-2 Hall-Sensor with Single-shunt Current Sampling

1.5 Functional Block Diagram

1.5.1 FT8132 with Sensorless Control

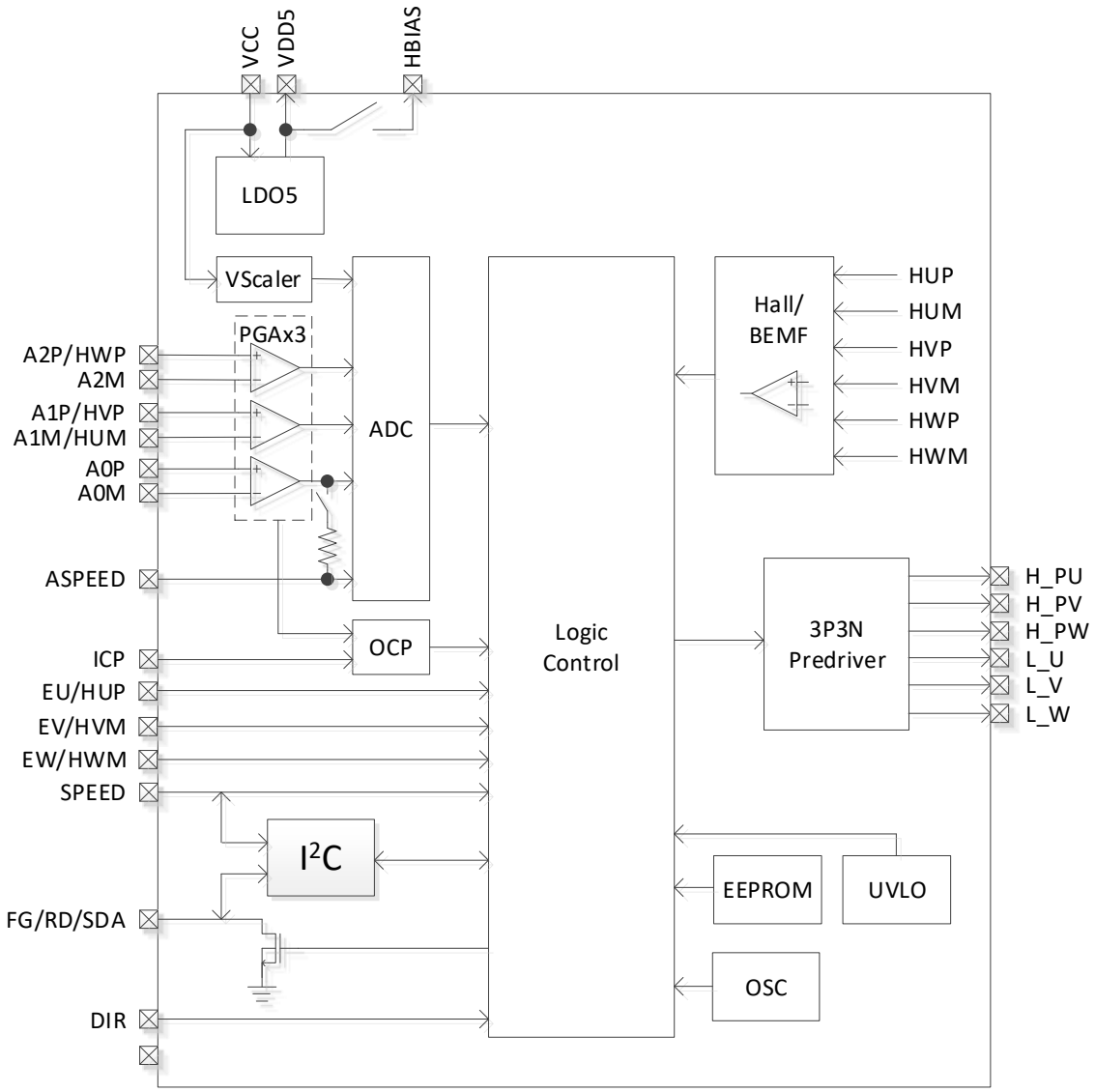


Figure 1-3 Functional Block Diagram of FT8132 with Sensorless Control

1.5.2 FT8132 with Hall-based Control

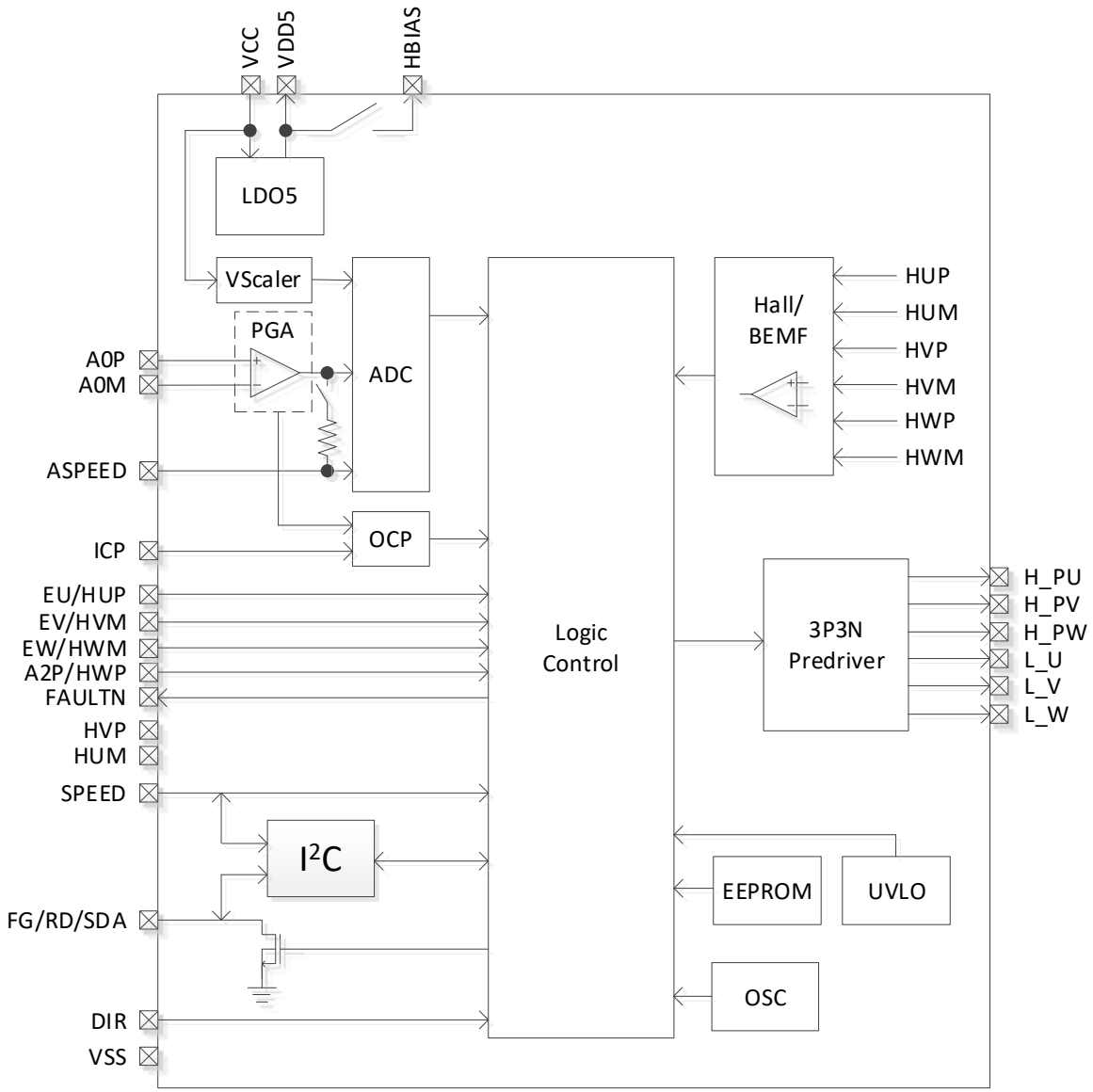


Figure 1-4 Functional Block Diagram of FT8132 with Hall-based Control

1.6 Pinout Diagram

1.6.1 FT8132Q QFN24

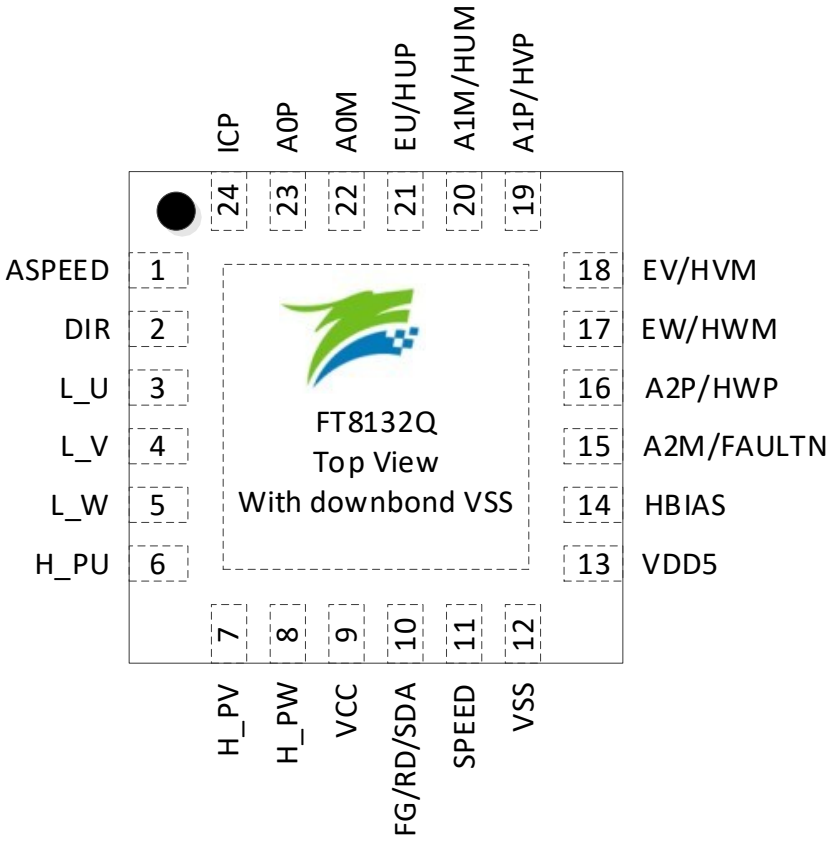


Figure 1-5 FT8132 QFN24 Pinout Diagram

1.6.2 FT8132S SSOP24

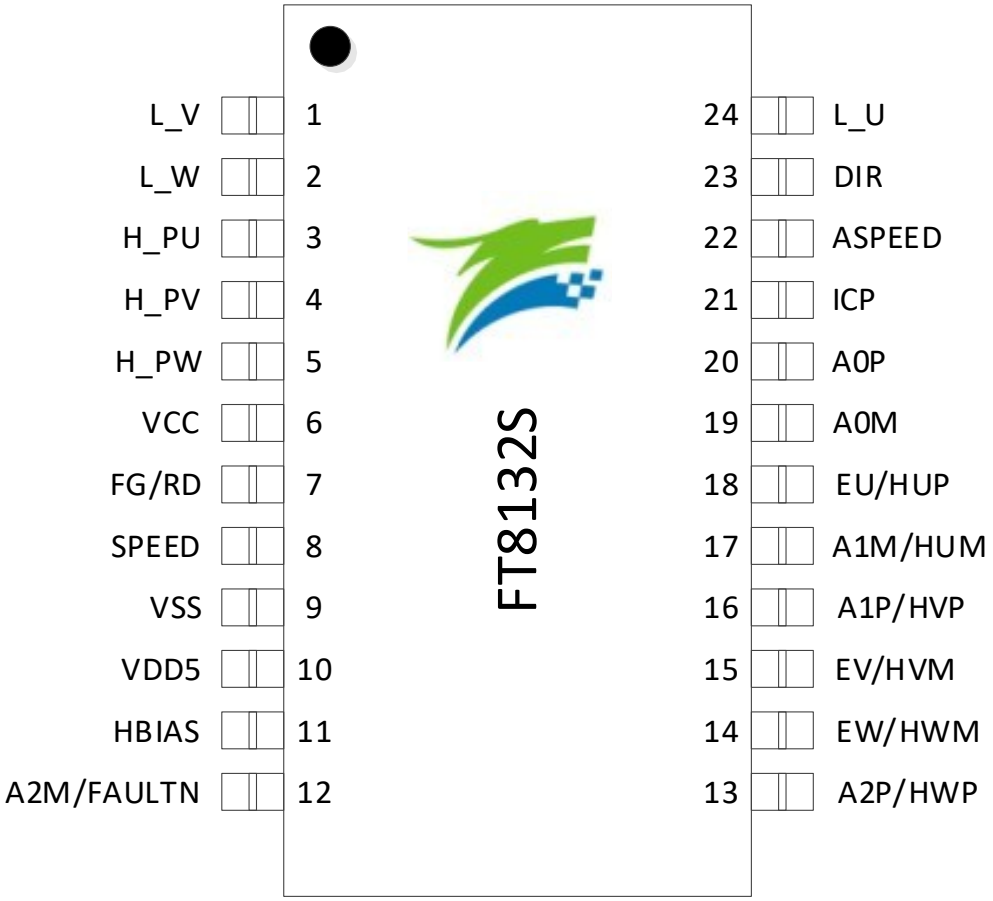


Figure 1-6 FT8132 SSOP24 Pinout Diagram

1.7 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

1.7.1 FT8132Q QFN24 Pins

Table 1-1 FT8132Q QFN24 Pin Descriptions

Pin	FT8132Q QFN24	IO Type	Description
ASPEED	1	AI	Analog voltage input for motor speed regulation
DIR	2	DI	Motor rotation control, with built-in pull-up resistor 0: Reverse rotation. The output phase sequence is U --> W --> V. 1: Forward rotation. The output phase sequence is U --> V --> W.
L_U	3	DO	3P3N pre-driver U-phase low-side output, with built-in 25kΩ pull-down resistor
L_V	4	DO	3P3N pre-driver V-phase low-side output, with built-in 25kΩ pull-down resistor
L_W	5	DO	3P3N pre-driver W-phase low-side output, with built-in 25kΩ pull-down resistor
H_PU	6	DO	3P3N pre-driver U-phase high-side output, with built-in 50kΩ pull-up resistor
H_PV	7	DO	3P3N pre-driver V-phase high-side output, with built-in 50kΩ pull-up resistor
H_PW	8	DO	3P3N pre-driver W-phase high-side output, with built-in 50kΩ pull-up resistor
VCC	9	P	Power supply. The input voltage range is 6V ~ 28V, with a more than 10μF capacitor connected to ground
FG/RD/ SDA	10	DO/ DB	Motor speed signal or motor block indication, with collector open-drain output I^2C SDA; Collector open-drain output
SPEED	11	DI	Input of PWM or CLOCK mode based speed regulation
VSS	12	P	Ground
VDD5	13	P	5V LDO output with a 1μF ~ 4.7μF capacitor connected to ground
HBIAS	14	DO	Hall bias power supply, internally connected to VDD5 via a switch
A2M/ FAULTN	15	AI/ DO	AMP2 negative input Fault output signal, with collector open-drain output
A2P/ HWP	16	AI/ AI	AMP2 positive input Positive input of W-phase Hall-Sensor
EW/ HWM	17	AI/ AI	W-phase BEMF voltage input Negative input of W-phase Hall-Sensor or input of W-phase Hall-IC
EV/ HVM	18	AI/ AI	V-phase BEMF voltage input Negative input of V-phase Hall-Sensor or input of V-phase Hall-IC
A1P/ HVP	19	AI/ AI	AMP1 positive input Positive input of V-phase Hall-Sensor

Pin	FT8132Q QFN24	IO Type	Description
A1M/ HUM	20	AI/ AI	AMP1 negative input Negative input of U-phase Hall-Sensor
EU/ HUP	21	AI/ AI	U-phase BEMF voltage input Positive input of U-phase Hall-Sensor or input of U-phase Hall-IC
A0M	22	AI	AMP0 negative input
A0P	23	AI	AMP0 positive input
ICP	24	AI	Input of overcurrent protection

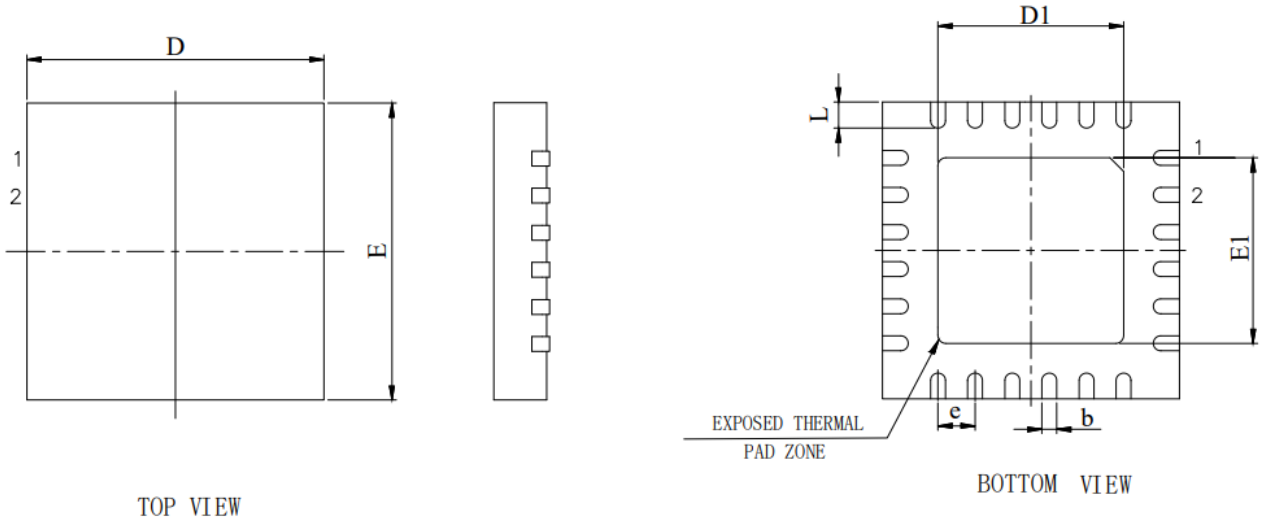
1.7.2 FT8132S SSOP24 Pins

Table 1-2 FT8132 SSOP24 Pin Descriptions

Pin	FT8132S SSOP24	IO Type	Description
L_V	1	DO	3P3N pre-driver V-phase low-side output, with built-in 25kΩ pull-down resistor
L_W	2	DO	3P3N pre-driver W-phase low-side output, with built-in 25kΩ pull-down resistor
H_PU	3	DO	3P3N pre-driver U-phase high-side output, with built-in 50kΩ pull-up resistor
H_PV	4	DO	3P3N pre-driver V-phase high-side output, with built-in 50kΩ pull-up resistor
H_PW	5	DO	3P3N pre-driver W-phase high-side output, with built-in 50kΩ pull-up resistor
VCC	6	P	Power supply. The input voltage range is 6V ~ 28V, with a more than 10μF capacitor connected to ground
FG/RD/ SDA	7	DO/ DB	Motor speed signal or motor block indication, with collector open-drain output I^2C SDA; Collector open-drain output
SPEED	8	DI	Input of PWM or CLOCK mode based speed regulation
VSS	9	P	Ground
VDD5	10	P	5V LDO output with a 1μF ~ 4.7μF capacitor connected to ground
HBIAS	11	DO	Hall bias power supply, internally connected to VDD5 via a switch
A2M/ FAULTN	12	AI/ DO	AMP2 negative input Fault output signal, with collector open-drain output
A2P/ HWP	13	AI/ AI	AMP2 positive input Positive input of W-phase Hall-Sensor
EW/ HWM	14	AI/ AI	W-phase BEMF voltage input Negative input of W-phase Hall-Sensor or input of W-phase Hall-IC
EV/ HVM	15	AI/ AI	V-phase BEMF voltage input Negative input of V-phase Hall-Sensor or input of V-phase Hall-IC
A1P/ HVP	16	AI/ AI	AMP1 positive input Positive input of V-phase Hall-Sensor
A1M/ HUM	17	AI/ AI	AMP1 negative input Negative input of U-phase Hall-Sensor
EU/ HUP	18	AI/ AI	U-phase BEMF voltage input Positive input of U-phase Hall-Sensor or input of U-phase Hall-IC
A0M	19	AI	AMP0 negative input
A0P	20	AI	AMP0 positive input
ICP	21	AI	Input of overcurrent protection
ASPEED	22	AI	Analog voltage input for motor speed regulation
DIR	23	DI	Motor rotation control, with built-in pull-up resistor 0: Reverse rotation. The output phase sequence is U --> W --> V. 1: Forward rotation. The output phase sequence is U --> V --> W.
L_U	24	DO	3P3N pre-driver U-phase low-side output, with built-in 25kΩ pull-down resistor

2 Package Information

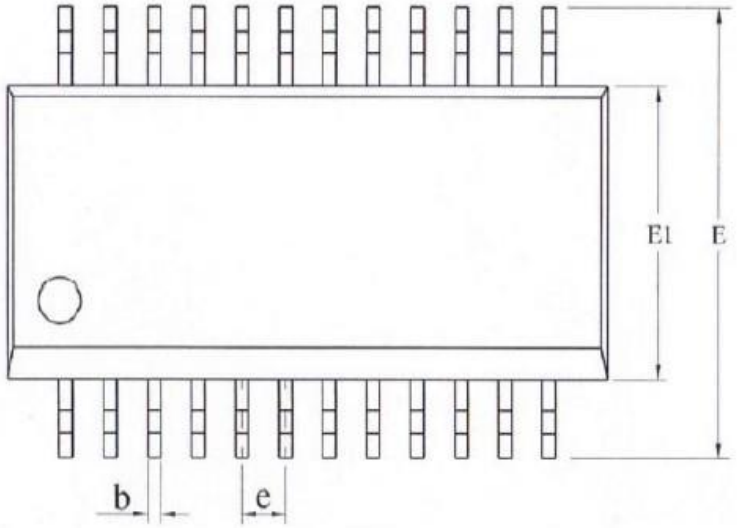
2.1 FT8132Q QFN24_4X4

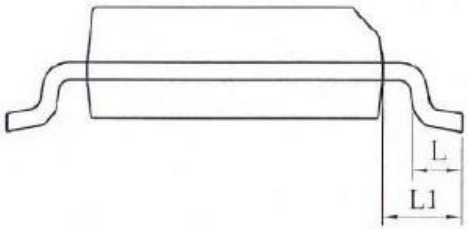


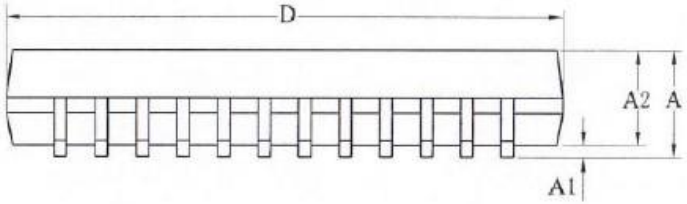
QFN24L			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
E	3.9	4	4.1
D	3.9	4	4.1
E1	2.2		2.6
D1	2.2		2.6
L	0.3	0.4	0.5
e		0.5	
b	0.18	0.25	0.3

Figure 2-1 FT8132Q QFN24_4X4 Package Drawings and Dimensions

2.2 FT8132S SSOP24_8.65X3.9







SSOP24			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A			1.75
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
D	8.55	8.65	8.75
E	5.8	6	6.2
E1	3.8	3.9	4
L	0.5		0.8
L1		1.05	
e		0.635	
b	0.23		0.31

Figure 2-2 FT8132S SSOP24_8.65X3.9 Package Drawings and Dimensions

3 Ordering Information

Table 3-1 Model Selections

Model	Power Supply (V)	Driver Interface	Control Features						Protection Features						Operating Temperature T_j(℃)	Lead-free	Package
			Driver Type	Speed Regulation			Forward and Reverse Rotation	Initial Position Detection	OCP	UVLO	OVLO	MLP	HALLERR	Phase Loss Protection			
				I²C	PWM / CLOCK	Analog Voltage											
FT8132Q	6 ~ 28	3P3N Pre-driver	Sensored & Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	√	-40 ~ 150	√	QFN24 (4x4mm)
FT8132S	6 ~ 28	3P3N Pre-driver	Sensored & Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	√	-40 ~ 150	√	SSOP24 (8.65x3.9mm)

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Operating Junction Temperature T_j		-40	-	150	℃
Storage Temperature T_{stg}		-55	-	150	℃
VCC to VSS Voltage		-0.3	-	30	V
VDD5 to VSS Voltage		-0.3	5	6.5	V
FG to VSS Voltage		-0.3	-	VCC + 0.3	V
H_PU/H_PV/H_PW to VSS Voltage		-0.3	-	VCC + 0.3	V
L_U/L_V/L_W to VSS Voltage		-0.3	-	VCC + 0.3	V
DIR/ASPEED/ICP/A0P/A0M/ EU/A1M/A1P/EV/EW/A2P/ A2M/HBIAS/SPEED to VSS Voltage		-0.3	-	VDD5 + 0.3	V

Note: Stress values greater than "Absolute Maximum Ratings" listed above may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

4.2 Global Electrical Characteristics

Table 4-2 Global Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC Operating Voltage		6	-	28	V
VDD5 Operating Voltage	T_A = -40℃ ~ 85℃	4.8	5	5.2	V
VCC Operating Current I_{VCC}	T_A = -40℃ ~ 85℃	-	15	25	mA
VDD5 Load Current	T_A = -40℃ ~ 85℃	-	-	10	mA
VCC Sleep-mode Current $I_{VCC\text{-}sleep}$	T_A = -40℃ ~ 85℃	-	50	100	μA

4.3 Protection Electrical Characteristics

Table 4-3 Protection Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCC UVLO Lockout Voltage V_{UVLO}		4.8	5.4	6	V
VCC UVLO Hysteresis Voltage $V_{UVLO\text{-}HYS}$		-	0.4	-	V

4.4 IO Electrical Characteristics (DIR/SPEED/FG)

Table 4-4 Electrical Characteristics (DIR/SPEED/FG)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage V_{IH}		0.6*VDD5	-	-	V
Low-level Input Voltage V_{IL}		-	-	0.2*VDD5	V
SPEED/DIR/A1P Pull-up Resistor		-	33	-	kΩ
SPEED Pull-down Resistor		-	30	-	kΩ
EW/EV/EU/A2P/A2M Pull-up Resistor		-	5.6	-	kΩ

4.5 PWM/CLOCK Input Frequency

Table 4-5 PWM/CLOCK Input Frequency

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWM Input Frequency		100	-	100k	Hz
CLOCK Input Frequency		20	-	1400	Hz

4.6 Pre-driver Electrical Characteristics

Table 4-6 Pre-driver Electrical Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-side Output Source Current		-	150	-	mA
High-side Output Sink Current		-	90	-	mA
Low-side Output Source Current		-	150	-	mA
Low-side Output Sink Current		-	180	-	mA
Rise Time of High-side Output	1nF load, from 10% to 90%	-	25	-	ns
Fall Time of High-side Output	1nF load, from 90% to 10%	-	90	-	ns
Rise Time of Low-side Output	1nF load, from 10% to 90%	-	115	-	ns
Fall Time of Low-side Output	1nF load, from 90% to 10%	-	60	-	ns

4.7 Speed Control with Analog Voltage

Table 4-7 Speed Control with Analog Voltage

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ASPEED Input Voltage		0	-	VDD5	V

4.8 Package Thermal Resistance

Table 4-8 QFN24 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Temperature Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	50	°C/W
Junction-to-case Temperature Thermal Resistance θ_{JC}[1]	JEDEC standard, 2S2P PCB	25	°C/W

Note:

[1] The actual measurements may vary depending on the conditions.

Table 4-9 SSOP24 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Temperature Thermal Resistance θ_{JA}[1]	JEDEC standard, 2S2P PCB	85	℃/W

Note:

[1] The actual measurements may vary depending on the conditions.

5 Function Description

5.1 VDD5

VDD5 is applied to internal digital logic and analog circuits only, and cannot be used for external circuits. A capacitor of 1μF or above shall be added at VREF pin to stabilize the power supply.

5.2 HBIAS

HBIAS is Hall bias power supply which is internally connected to VDD5 through a configurable switch. The maximum load capacity is 10mA.

5.3 DIR

Forward or reverse direction control (DIR) pin is used to reverse motor rotation by changing the DIR level. Pull-ups make the pin state as "High" (or "1") by default.

5.4 ICP

ICP pin is used for the input of sampling current when overcurrent protection is enabled.

5.5 ASPEED

Analog voltage for motor speed regulation (ASPEED) pin is used to input analog voltage for speed regulation.

5.6 SPEED

Speed control (SPEED) pin is used to input duty cycle for speed regulation depending on the settings. In addition, SPEED pin serves as the clock line (SCL) for I^2C communication.

5.7 FG/RD/SDA

Speed detection and fault indication (FG/RD/SDA) pin is an open-drain output. When this pin is set to FG, it outputs speed feedback signal to indicate rotation speed of the motor, and when it is set to RD, it outputs high-level signal to indicate the fault state. In addition, the pin serves as the data line (SDA) for I^2C communication.

Configuring FG/RD/SDA to FG outputs FG signal, that is, FG/RD/SDA pin is selected to output FG signal. The output frequency of FG signal is determined by FGDIV (frequency division coefficient) and FGMUL (frequency multiplication coefficient). FGMUL can be set as 1, 2, 3 and 4, while FGDIV as 1, 1/3, 1/4 and 1/5. k (coefficient of output frequency) = FGMUL*FGDIV.

Table 5-1 FG Configurations

Coefficient of Output Frequency (k)		**FGMUL**			
		1	**2**	**3**	**4**
FGDIV	**1**	1	2	3	4
	1/3	1/3	2/3	3/3	4/3
	1/4	1/4	2/4	3/4	4/4
	1/5	1/5	2/5	3/5	4/5

The number of FG signals in one mechanical cycle is equal to pp*k (pp refers to pole-pair number of the motor).

Example: For a 4-pole-pair motor, if FGMUL is set as 3 and FGDIV as 1/4, that is, k = 3/4, three FG signals are displayed in one mechanical cycle (4 * 3/4).

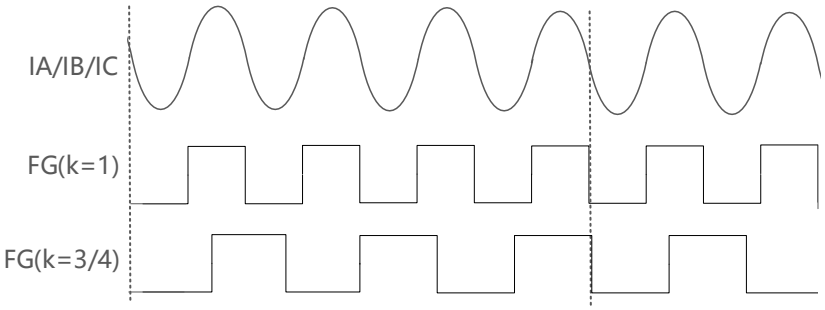


Figure 5-1 FG Output Waveforms When k = 1 and k= 3/4

In sensored mode, if FG3 or FG1 frequency multiplication to follow Hall output is configured, FG signals are output based on the corresponding settings. Otherwise, FG signals are output based on the configured FGDIV and FGMUL.

5.8 Speed Control

5.8.1 Speed Control Modes

The chip supports four types of speed control: PWM, analog voltage, I²C and CLOCK, and only one of them can be chosen at a time. If analog voltage is selected, voltage value input to the ASPEED pin controls the speed; if PWM or CLOCK is selected, duty cycle of PWM or CLOCK signal input to SPEED pin controls the speed; and if I²C is selected, SPEED pin serves as the clock line (SCL) and FG pin as the data line (SDA).

5.8.1.1 CLOCK Speed Regulation Mode

In this mode, SPEED pin serves as the input of reference PWM frequency, and motor speed changes with reference PWM frequency. FGMUL and FGDIV are used to set the factor between motor speed and reference PWM frequency: Motor Speed = (reference PWM frequency*60/pp)/(FGMUL*FGDIV).

Example: For a 5-pole-pair motor, if FGDIV is set as 1/3 and FGMUL as 2 (i.e., k = 2/3), and the reference PWM frequency is 100Hz, then motor speed = (100Hz*60/5) / (2/3) = 1800rpm. In this case, the output frequency from FG pin is determined by FGDIV and FGMUL.

5.8.2 Speed Control Curve

The control waveform is presented as below, where x-coordinate refers to the duty cycle of PWM input (In I²C control and analog control modes, the input can be converted to the corresponding PWM duty cycle.), and y-coordinate refers to the output duty cycle, which represents different physical quantities in different control modes.

The y-coordinate represents Duty in voltage-loop control mode. The multi-segment speed control curve is obtained by setting five output duty cycle reference points. The start point is determined by X_ON, and the maximum duty cycle PWM_X98 can be set as 98% or 100%. The three inflection points of speed regulation curve are fixed at 25%, 50% and 75%, and the corresponding output reference Y_ON, Y_25, Y_50, Y_75 and Y_MAX are configurable.

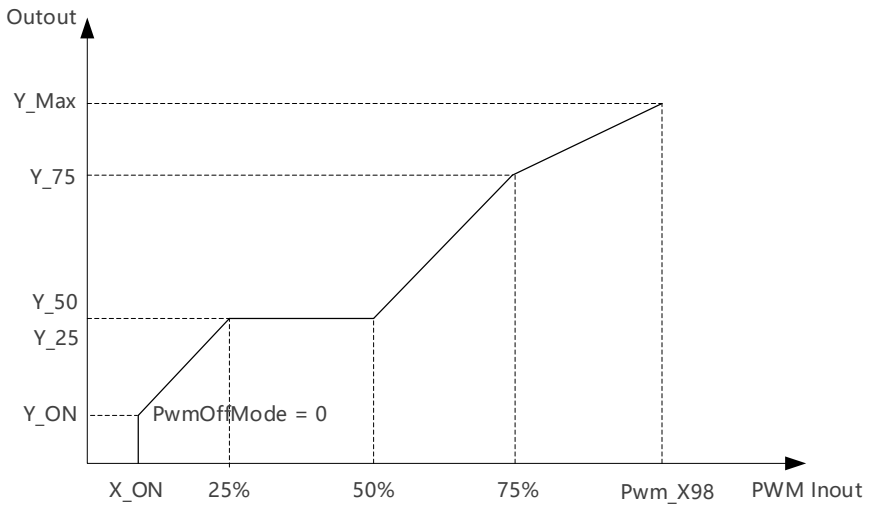


Figure 5-2 Output Curve in Voltage-loop Mode (PwmOffMode = 0)

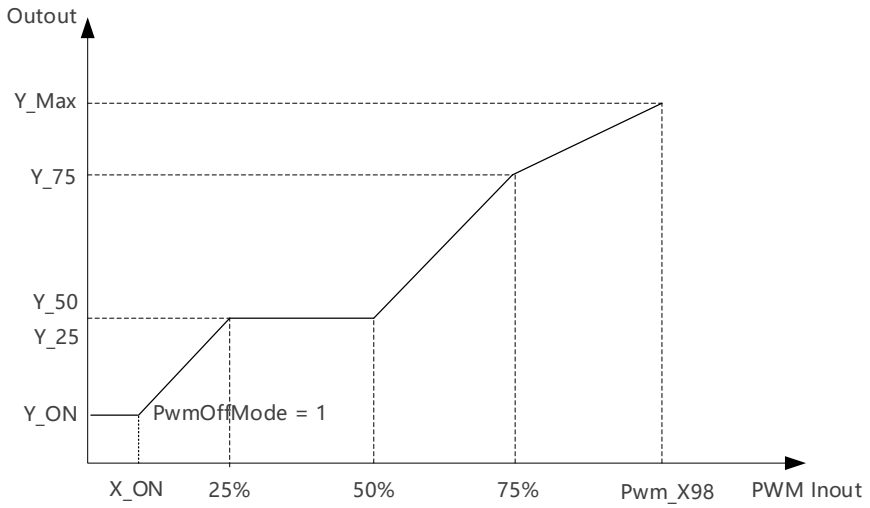


Figure 5-3 Output Curve in Voltage-loop Mode (PwmOffMode = 1)

When speed/current/power-loop is selected, y-coordinate represents motor speed/current/motor power. In this case, only Y_ON and Y_MAX are configurable, and the output of other points between them increases linearly as the input varies.

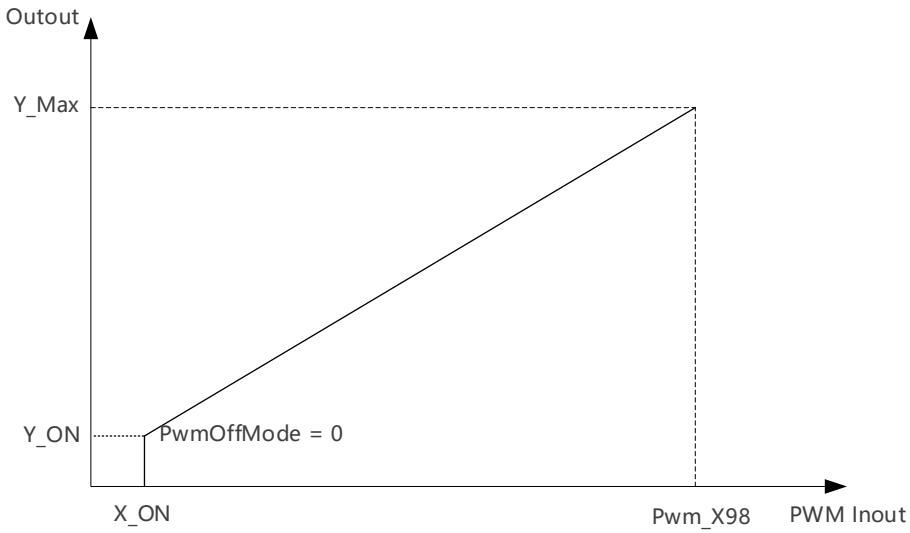


Figure 5-4 Output Curve in Speed/Current/Power-loop Mode (PwmOffMode = 0)

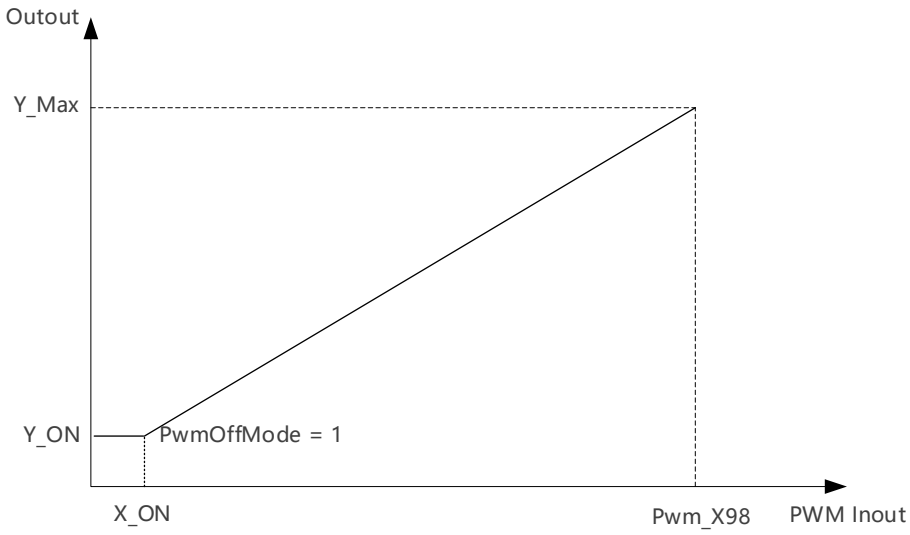


Figure 5-5 Output Curve in Speed/Current/Power-loop Mode (PwmOffMode = 1)

5.9 Lead Angle Curve

In sensored SVPWM control mode, lead angle curve corresponding to duty cycle of the voltage output is shown in Figure 5-6, where x-coordinate denotes duty cycle of the PWM voltage and y-coordinate represents the lead angle. The multi-stage lead angle curve is developed by setting lead angle at 9 points, which better fits the motor characteristics. Such 9 points are 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, 87.5% and 100%, respectively, and the maximum angle difference between each two adjacent points is 10.547°.

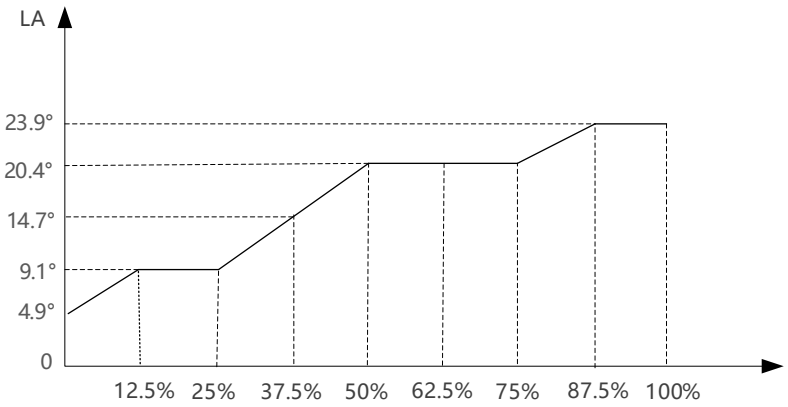


Figure 5-6 Lead Angle Curve

5.10 Sleep Mode

The motor enters sleep mode when the motor stays in stop state for 6 seconds.

Wakeup conditions: In I^2C speed control mode, the chip exits sleep mode after receiving the matched I^2C ID. In PWM or CLOCK speed control mode, if inverted input is disabled, the chip exits sleep mode when a high-level voltage is input to SPEED pin; and if inverted input is enabled, the chip exits sleep mode when a low-level voltage is input to SPEED pin. In analog voltage control mode, the chip exits sleep mode when the voltage of ASPEED pin is greater than 1.5V or when a high-level voltage is input to SPEED pin.

5.11 Soft-on and Soft-off

Soft-on feature gradually increases the current during start-up process, and soft-off feature gradually decreases the current during shut-down process. The two features protect the motor from abrupt startup or shutdown and reduce noise during operation.

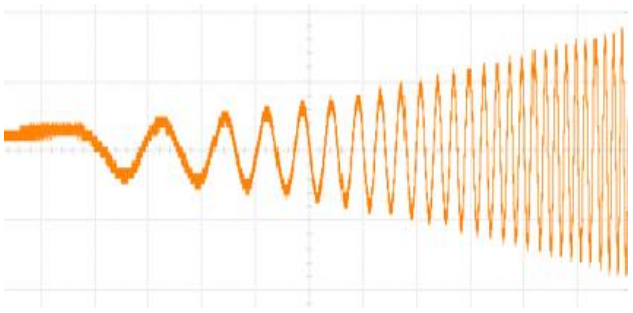


Figure 5-7 Soft-On Phase Current Wave

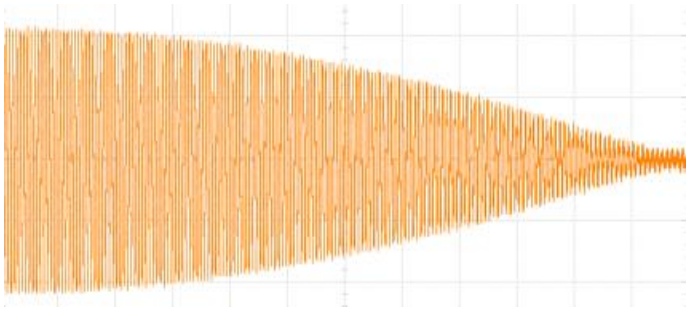


Figure 5-8 Soft-Off Phase Current Wave

5.12 Motor Lock Protection

Motor lock protection circuitry monitors operating state of the motor. When the conditions for motor lock are satisfied, the chip shuts down and waits for 6s to decide whether to restart (depending on software settings).

5.13 Phase Loss Protection

Phase loss protection circuitry monitors operating state of the motor. When the conditions for phase loss are satisfied, the chip shuts down and waits for 6s to decide whether to restart (depending on software settings).

5.14 Overcurrent Protection

When the sampling current exceeds the overcurrent protection threshold, the chip shuts down and waits for 6s to decide whether to restart (depending on software settings).

6 Revision History

Rev.	Description	Date	Prepared By
V0.1	Preliminary datasheet, translated from Chinese version 0.1	2022/01/04	Bruce Long/ Power Liao
V0.2	Added FT8132S SSOP24	2022/02/23	Bruce Long/ Power Liao
V0.3	Standardized document format	2022/03/27	Spring Wen
V0.4	Corrected some typing errors and standardized document format	2022/04/15	Black Li
V0.5	Updated descriptions in Copyright Notice and standardized document format	2022/06/09	Michelle Jiang
V1.0	1. Deleted descriptions on TSD features; removed the "Thermal" functional block in Figure 1-3 Functional Block Diagram of FT8132 with Sensorless Mode and Figure 1-4 Functional Block Diagram of FT8132 with Hall Effected Control; and deleted the parameters "Junction temperature T_{TSD}" and "Temperature hysteresis T_{TSD_HYS}" in Table 4-3 Protection Electrical Characteristics; 2. Proofread the overall document.	2023/05/15	Eric Deng
V1.1	1. Added descriptions on pull-down resistor or pull-down resistor of L_U, L_V, L_W, H_PU, H_PV and H_PW in 1.7 Pin Definitions; 2. Updated section 2 Package Information; 3. Deleted descriptions on overtemperature lock; 4. Standardized document format.	2023/10/12	Eric Deng
V1.2	Updated Figure 2-2 FT8132S SSOP24_8.65X3.9 Package Drawings and Dimensions.	2023/10/26	Eric Deng

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Fortior Technology (Shenzhen) Co., Ltd.

Room 203, 2/F, Building No.11, Keji Central Road 2,
Software Park, High-Tech Industrial Park, Shenzhen, P.R. China 518057
Tel: 0755-26867710
Fax: 0755-26867715
URL: http://www.fortiortech.com

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