Datasheet

250V Three-phase Gate Driver

ED6288

Fortior Technology Co., Ltd.

Contents

ED6288 250V Three-phase Gate Driver

1 System Introduction

1.1 Overview

ED6288 is an integrated circuit (IC) that integrates three independent half-bridge gate drivers. It is specially designed for high-voltage and high-speed drive MOSFETs and operates up to +250V.

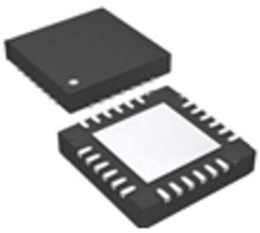
ED6288 supports under-voltage lockout (UVLO) feature, protecting the power device from operating with insufficient voltage.

ED6288 also provides cross-conduction prevention and deadtime insertion to effectively protect the power IC and prevent both MOSFETs of each half-bridge from switching on at the same time.

ED6288 has built-in input signal filtering module to avoid input noise interference.

1.2 Packages

TSSOP-20



QFN-24

1.3 Features

- Fully operational to +250V
- Power supply: 5V to 20V
- Three independent half-bridge drivers
- Output current: +1.5A/-1.8A
- 3.3V and 5V logic input compatible
- V_{CC}/V_{BS} UVLO
- Cross-conduction prevention logic
- 200ns deadtime
- Built-in input filtering module
- Matched propagation delay for high-side and low-side channels
- Outputs in phase with inputs

1.4 Applications

Motor drivers

1.5 Typical Application Diagram

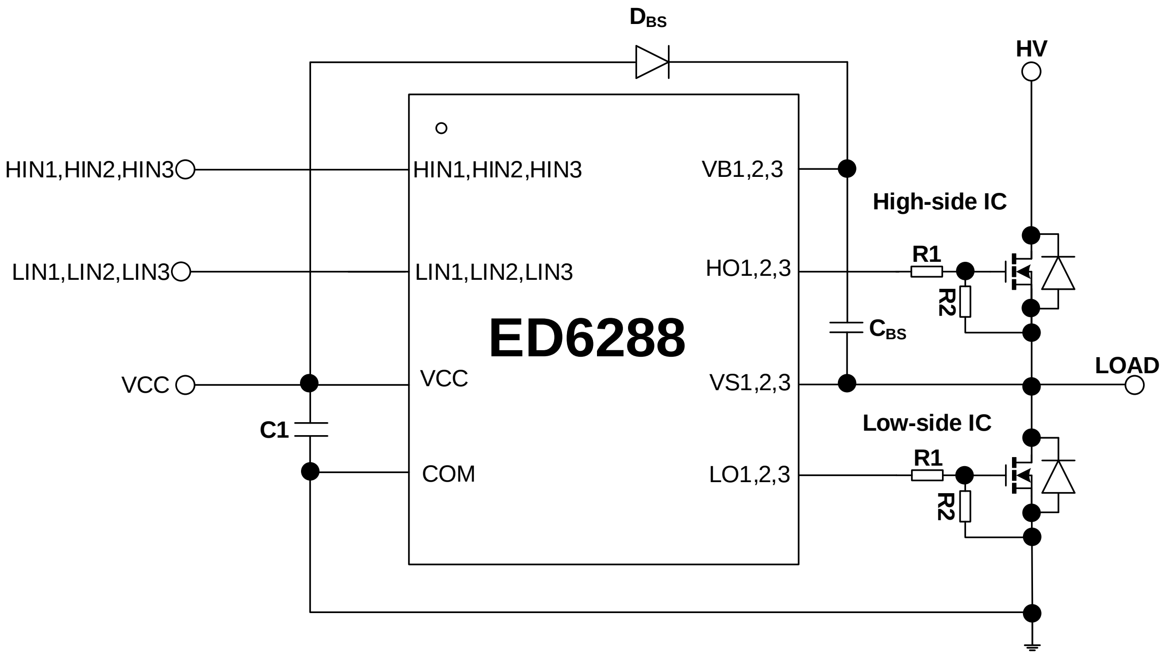


Figure 1-1 Typical Application Diagram of ED6288

C1: Power filter capacitor with 10μF optional. It shall be as close to the chip pin as possible.

R1: Gate drive resistor. The resistance depends on deadtime and the device being driven.

R2: MOS gate and source resistor.

D_{BS}: Bootstrap diode. Schottky diode with high reverse breakdown voltage and short recovery time is preferred.

C_{BS}: Bootstrap capacitor. Ceramic capacitor or tantalum capacitor is preferred. It shall be as close as possible to the chip pin.

Note: The above circuits and parameters are for reference only. The actual circuit shall be designed with the measured results.

1.6 Functional Block Diagram

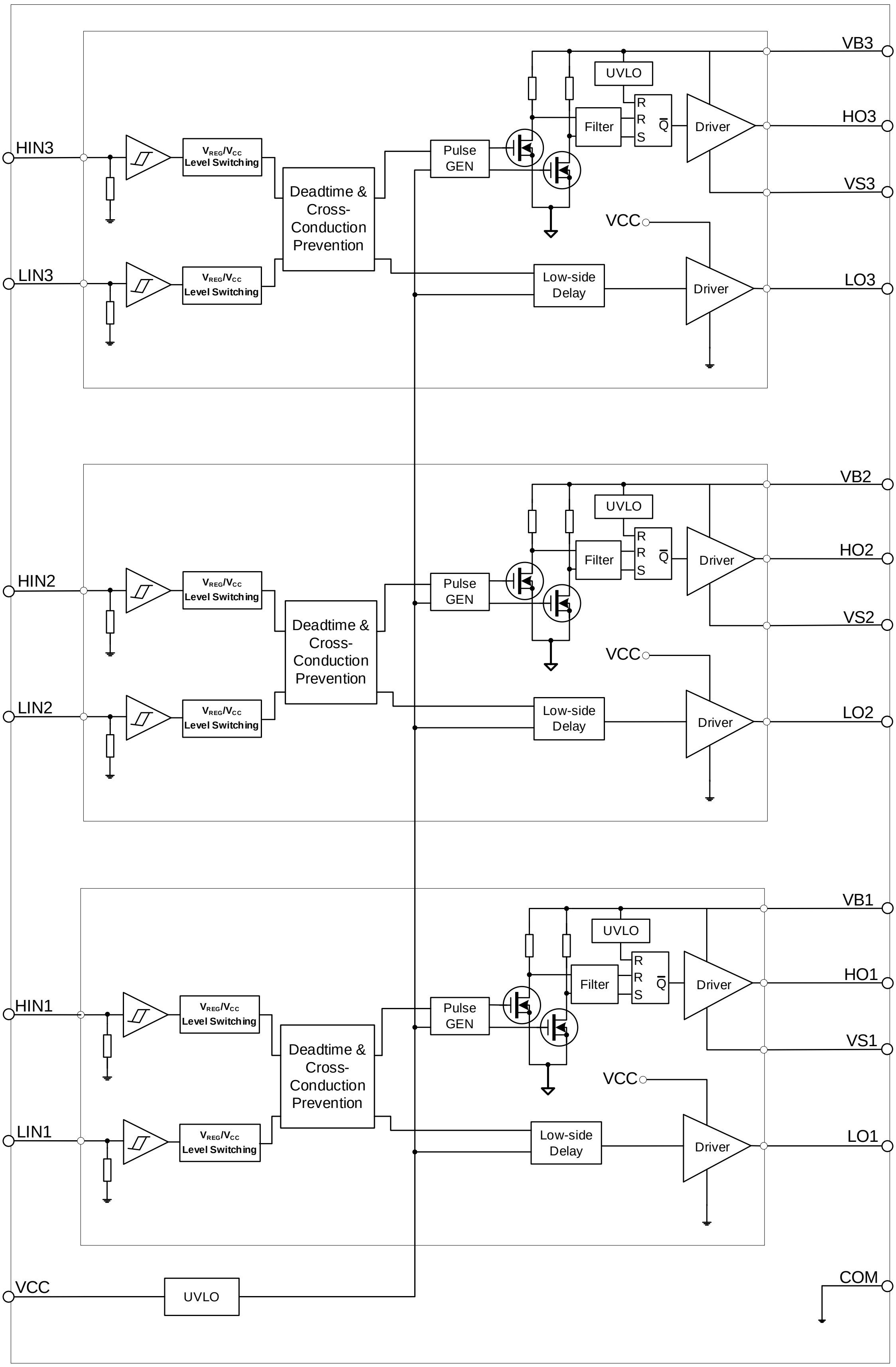


Figure 1-2 Functional Block Diagram of ED6288

1.7 Pin Definitions

1.7.1 ED6288T TSSOP20 Pin Diagram

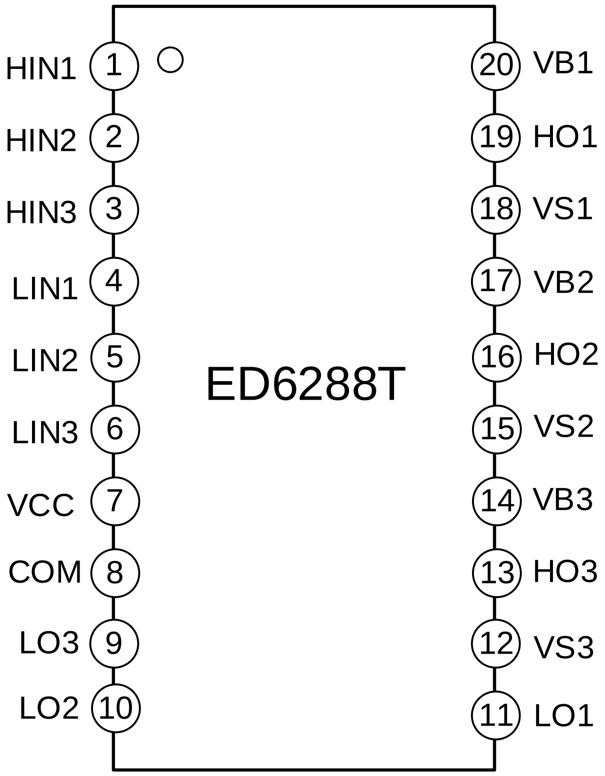


Figure 1-3 Pin Diagram of ED6288T TSSOP20

1.7.2 ED6288T TSSOP20 Pin Descriptions

Table 1-1 ED6288T TSSOP20 Pin Descriptions

Pin	Name	Description
1, 2, 3	HIN1, HIN2, HIN3	High-side Input
4, 5, 6	LIN1, LIN2, LIN3	Low-side Input
7	VCC	Low-side Power Supply
8	COM	Ground
9, 10, 11	LO3, LO2, LO1	Low-side Output
12, 15, 18	VS3, VS2, VS1	High-side Floating Offset Voltage
13, 16, 19	HO3, HO2, HO1	High-side Output
14, 17, 20	VB3, VB2, VB1	High-side Floating Absolute Voltage

1.7.3 ED6288Q QFN24 Pin Diagram

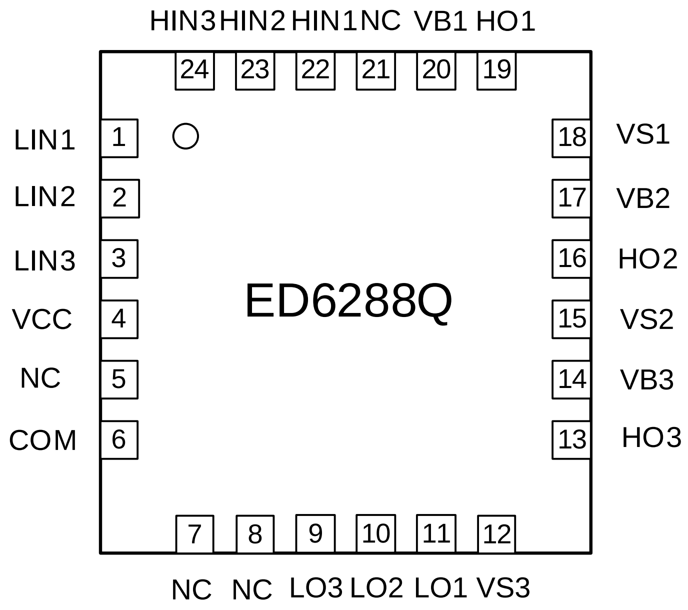


Figure 1-4 Pin Diagram of ED6288Q QFN24

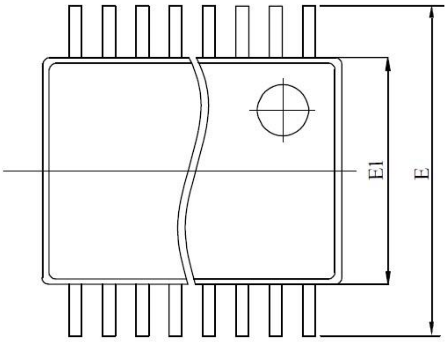
1.7.4 ED6288Q QFN24 Pin Descriptions

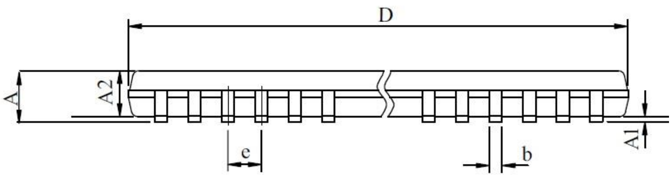
Table 1-2 ED6288Q QFN24 Pin Descriptions

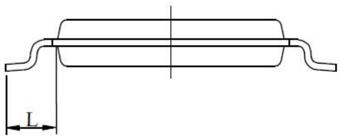
Pin	Name	Description
22, 23, 24	HIN1, HIN2, HIN3	High-side Input
1, 2, 3	LIN1, LIN2, LIN3	Low-side Input
4	VCC	Low-side Power Supply
6	COM	Ground
9, 10, 11	LO3, LO2, LO1	Low-side Output
12, 15, 18	VS3, VS2, VS1	High-side Floating Offset Voltage
13, 16, 19	HO3, HO2, HO1	High-side Output
14, 17, 20	VB3, VB2, VB1	High-side Floating Absolute Voltage
5, 7, 8, 21	NC	Not Connected

2 Package Information

2.1 ED6288T TSSOP20





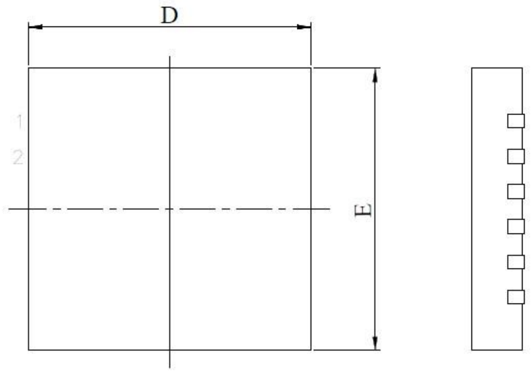


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A			1.2
A1	0.05		0.15
A2	0.8	1	1.05
E	6.2	6.4	6.6
E1	4.3	4.4	4.5
D	6.4	6.5	6.6
L	0.45	0.6	0.75
e		0.65	
b	0.2		0.28

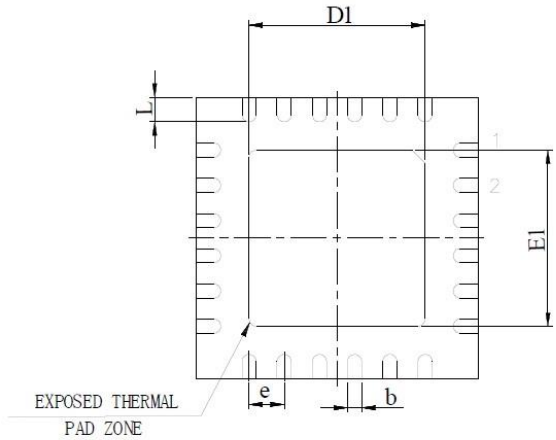
TSSOP20

Product Number	Package Type	Marking ID	Package Method	Quantity
ED6288T	TSSOP20	ED6288T	Tape & Reel	3000

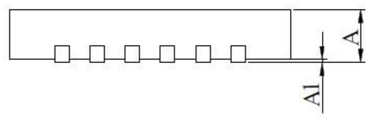
2.2 ED6288Q QFN24



TOP VIEW



BOTTOM VIEW



SIDE VIEW

QFN24L			
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0		0.05
E	3.9	4	4.1
D	3.9	4	4.1
E1	2.55		2.8
D1	2.55		2.8
L	0.3	0.4	0.5
e		0.5	
b	0.2		0.3

Product Number	Package Type	Marking ID	Package Method	Quantity
ED6288Q	QFN24	ED6288Q	Tape & Reel	3000

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

(All pins are referenced to COM unless otherwise specified)

Parameter		Symbol	Min. ~ Max.	Unit
High-side Floating Absolute Voltage		$V_{B1,2,3}$	-0.3～275	V
High-side Floating Offset Voltage		$V_{S1,2,3}$	$V_{B1,2,3}$-25～$V_{B1,2,3}$+0.3	V
High-side Output Voltage		$V_{HO1,2,3}$	$V_{S1,2,3}$-0.3～$V_{B1,2,3}$+0.3	V
Low-side Power Supply		V_{CC}	-0.3～25	V
Low-side Output Voltage		$V_{LO1,2,3}$	-0.3～V_{CC}+0.3	V
Logic Input Voltage (HIN, LIN)		V_{IN}	-0.3～V_{CC}+0.3	V
Swing Rate of Offset Voltage		dV_S/dt	≤50	V/ns
Power Dissipation @ T_A≤25°C	TSSOP20	P_D	≤1.25	W
	QFN24		≤3.0	
Junction-to-ambient Thermal Resistance	TSSOP20	R_{thJA}	≤100	°C/W
	QFN24		≤42	
Junction Temperature		T_j	≤150	°C
Storage Temperature		T_{stg}	-55～150	°C

Notes:

- In any case, power dissipation shall not exceed P_D.
- The chip may get damaged if it operates under voltages above the absolute maximum ratings.

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions[1]

(All voltages are referenced to COM unless otherwise specified)

Parameter	Symbol	Min.	Max.	Unit
High-side Floating Absolute Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$ + 5.0	$V_{S1,2,3}$ + 20	V
High-side Floating Offset Voltage[2]	$V_{S1,2,3}$	COM-4[3]	250	V
High-side Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low-side Power Supply	V_{CC}	5.0	20	V
Low-side Output Voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic Input Voltage (HIN, LIN)	V_{IN}	0	V_{CC}	V
Ambient Temperature	T_A	-40	125	°C

Notes:

[1] The reliability may get affected if the chip operates in an environment that exceeds the recommended conditions for a long period of time.

[2] The high-side floating offset voltage V_S is tested with 15V bias voltage.

[3] HO works normally when $V_{S1,2,3}$ ranges from (COM-4V) to 250V.

3.3 Static Electrical Characteristics

Table 3-3 Static Electrical Characteristics

(T_A =25°C, V_{CC}=$V_{BS1,2,3}$=15V and V_S=COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Threshold Voltage	V_{IH}		2.7	-	-	V
Low-level Input Threshold Voltage	V_{IL}		-	-	0.8	V
V_{CC} UVLO Threshold Voltage	V_{CCUV+}		4.2	4.6	5.0	V
V_{CC} UVLO Reset Voltage	V_{CCUV-}		3.9	4.3	4.7	V
V_{CC} UVLO Hysteresis Voltage	V_{CCUVH}		0.2	0.3	-	V
V_{BS} UVLO Threshold Voltage	V_{BSUV+}		4.2	4.6	5.0	V
V_{BS} UVLO Reset Voltage	V_{BSUV-}		3.9	4.3	4.7	V
V_{BS} UVLO Hysteresis Voltage	V_{BSUVH}		0.2	0.3	-	V
Leakage Current of Floating Power Supply	I_{LK}	$V_{B1,2,3}$=$V_{S1,2,3}$ =250V	-	0.1	5.0	μA
V_{BS} Quiescent Current	I_{QBS}	V_{IN}=0V or 5V	-	180	270	μA
V_{BS} Polyphase Current	I_{PBS}	$f_{HIN1,2,3}$=20kHz	-	180	270	μA
V_{CC} Quiescent Current	I_{QCC}	V_{IN} =0V or 5V	-	330	500	uA
V_{CC} Polyphase Current	I_{PCC}	$f_{LIN1,2,3}$=20kHz	-	330	500	uA
LIN High-level Input Bias Current	I_{LIN+}	V_{LIN}=5V	-	25	40	μA
LIN Low-level Input Bias Current	I_{LIN-}	V_{LIN}=0V	-	-	1	μA
HIN High-level Input Bias Current	I_{HIN+}	V_{HIN}=5V	-	25	40	μA
HIN Low-level Input Bias Current	I_{HIN-}	V_{HIN}=0V	-	-	1	μA
Input Pull-down Resistance	R_{IN}		140	200	260	KΩ
High-level Output Voltage	V_{OH}	I_O=100mA	-	0.6	0.9	V
Low-level Output Voltage	V_{OL}	I_O=100mA	-	0.3	0.45	V
High-level Output Short-circuit Pulse Current	I_{OH}	V_O=0V, V_{IN}=5V, PWD≤10μs	1.1	1.5	1.9	A
Low-level Output Short-circuit Pulse Current	I_{OL}	V_O=15V, V_{IN}=0V, PWD≤10μs	1.3	1.8	2.3	A
V_S Negative Offset Voltage	V_{SN}		-	-6.0	-	V

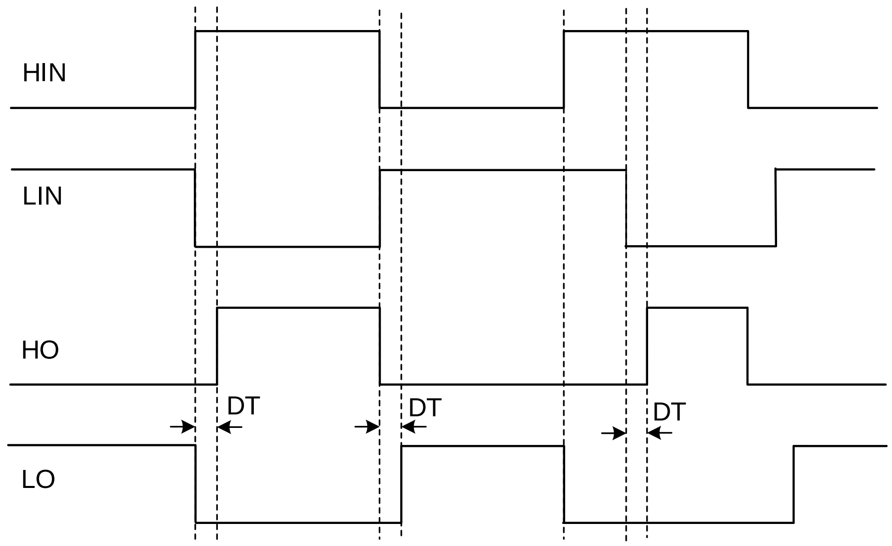
3.4 Dynamic Electrical Characteristics

Table 3-4 Dynamic Electrical Characteristics

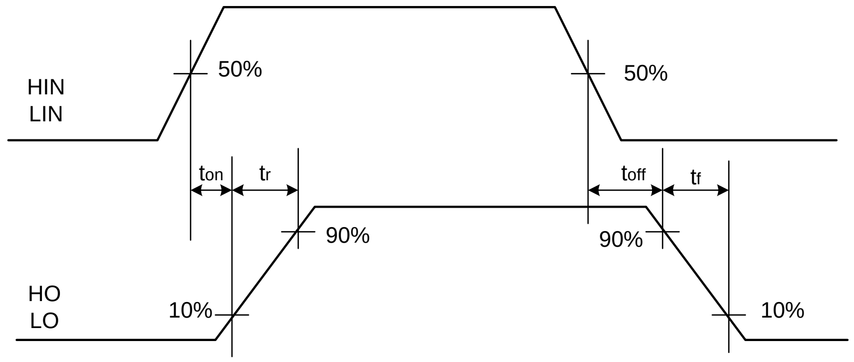
(T_A=25°C, V_{CC}=$V_{BS1,2,3}$=15V and V_S=COM unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Propagation Delay	t_{on}		-	300	450	ns
Turn-off Propagation Delay	t_{off}		-	100	160	ns
Turn-on Rise Time	t_r	C_L=1000pF	-	12	25	ns
Turn-off Fall Time	t_f	C_L=1000pF	-	12	25	ns
High-low Side Delay Match	MT		-	-	30	ns
Deadtime	DT		100	200	300	ns

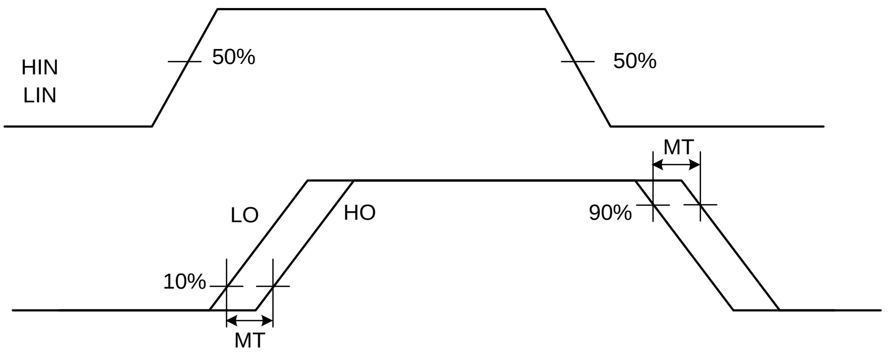
4 Logic Function Timing Diagram



5 Propagation Delay Test Standards

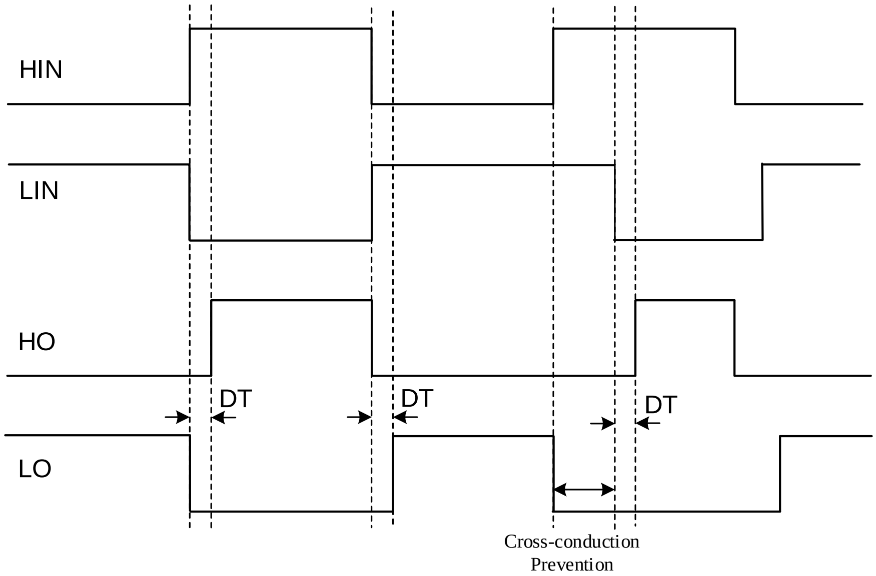


6 Propagation Delay Matching Test Standards



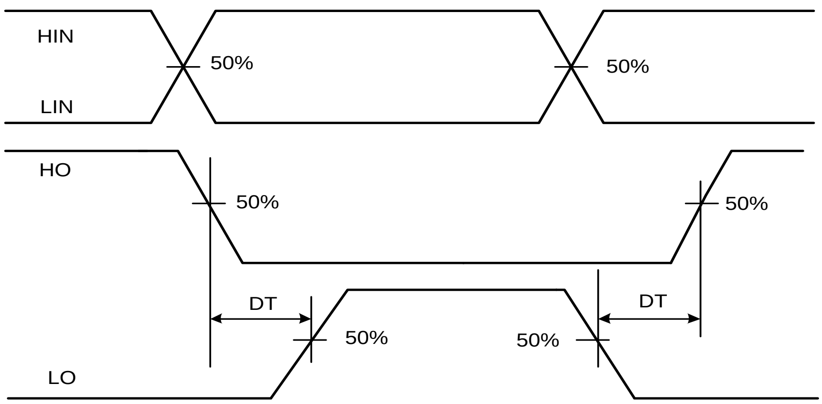
7 Cross-conduction Prevention

A protection circuit is specially designed inside the chip to enable cross-conduction prevention feature, which effectively prevents MOSFETs from damage when high-side and low-side input signals are interfered. The figure below shows how the protection circuit works.



8 Deadtime

The chip is designed with dedicated deadtime protection circuit. Both the high-side and low-side outputs are set to LOW during the deadtime. This feature prevents both MOSFETs of each half-bridge from switching on at the same time. The following figure shows the timing relation between deadtime, input signal and output signal.



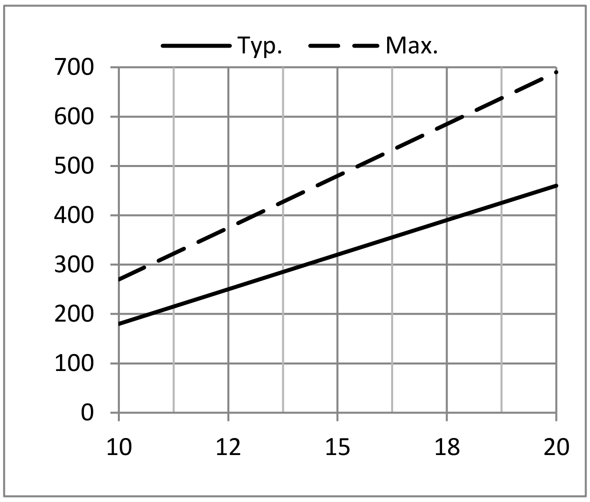


Figure 1A V_{CC} Supply Current vs V_{CC} Supply Voltage

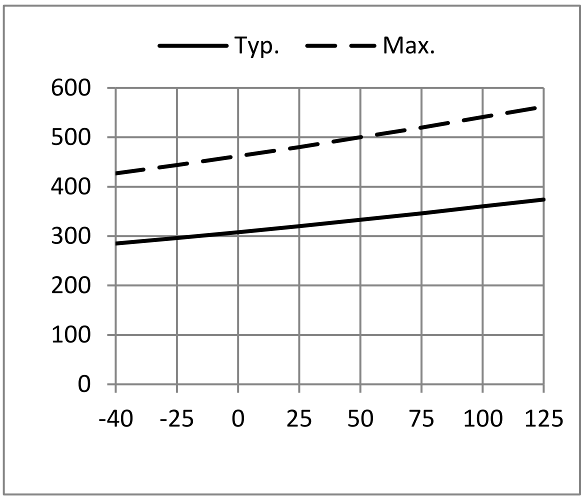


Figure 1B V_{CC} Supply Current vs Temperature

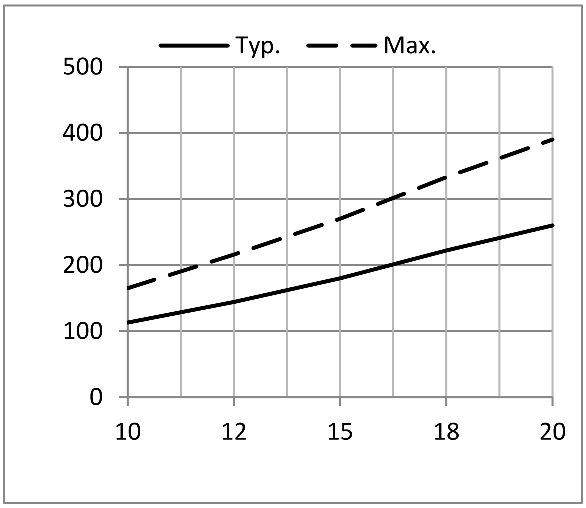


Figure 2A V_{BS} Supply Current vs V_{BS} Supply Voltage

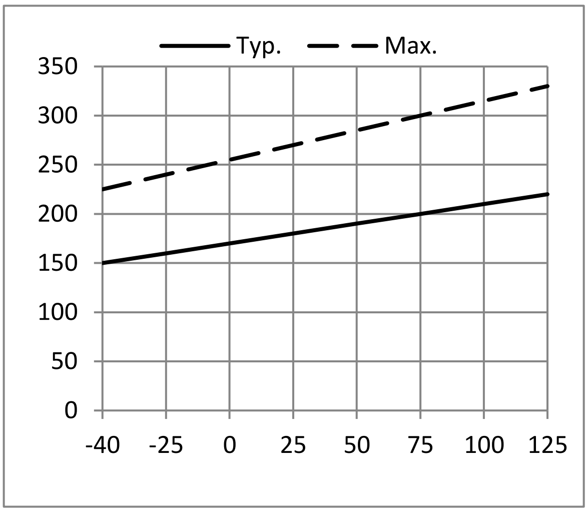


Figure 2B V_{BS} Supply Current vs Temperature

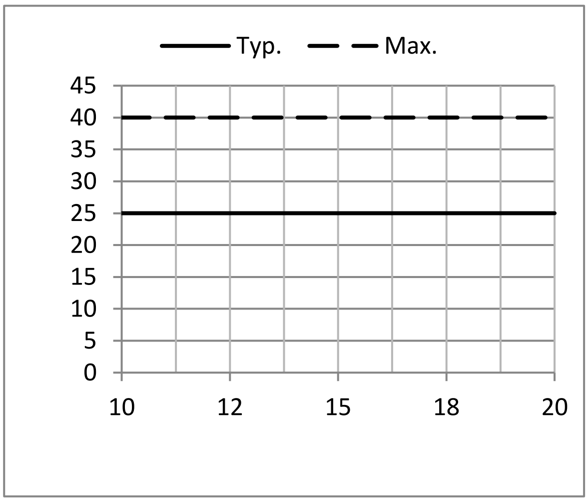


Figure 3A High-level Input Bias Current vs Supply Voltage

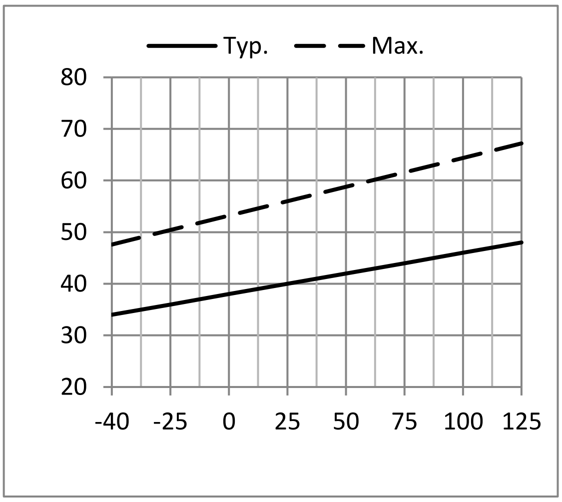


Figure 3B High-level Input Bias Current vs Temperature

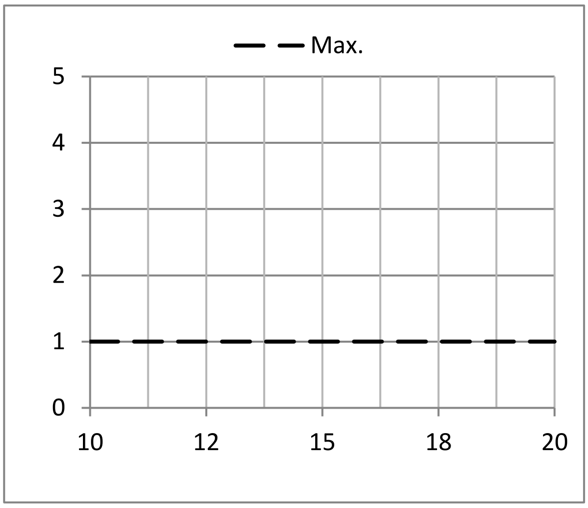


Figure 4A Low-level Input Bias Current vs Supply Voltage

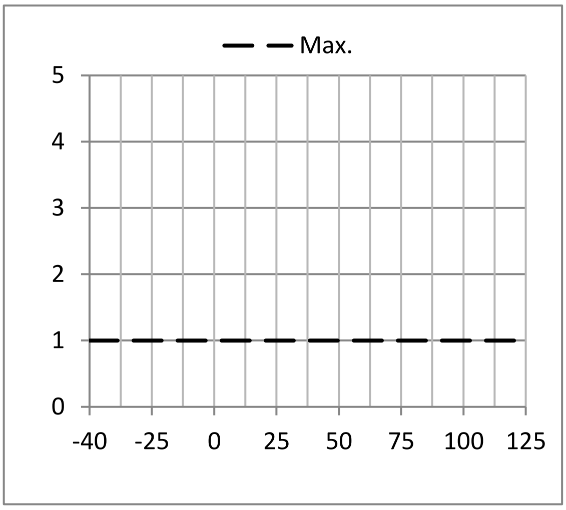


Figure 4B Low-level Input Bias Current vs Temperature

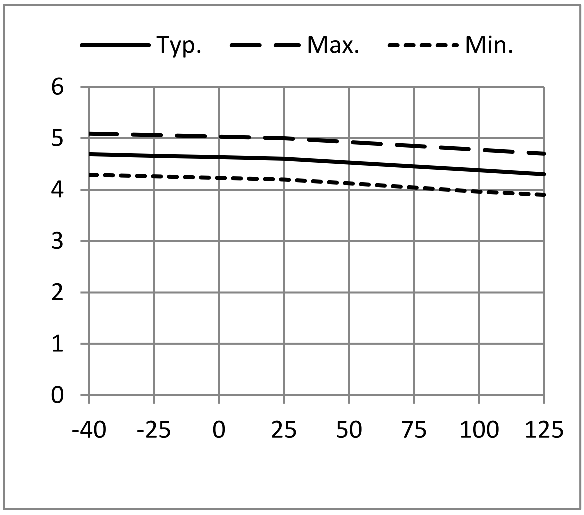


Figure 5A V_{CC} UVLO Threshold Voltage vs Temperature

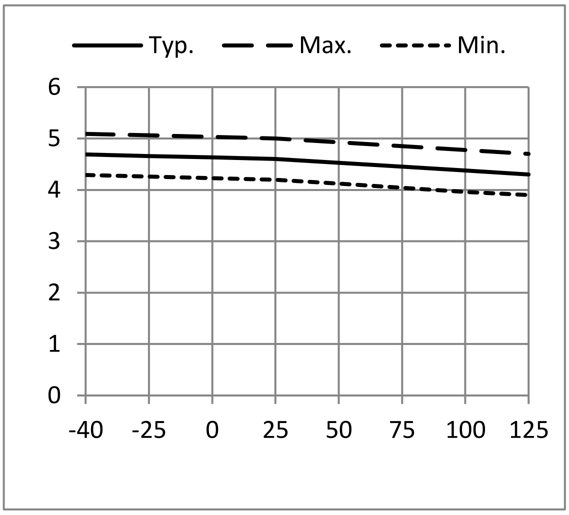


Figure 5B V_{CC} UVLO Reset Voltage vs Temperature

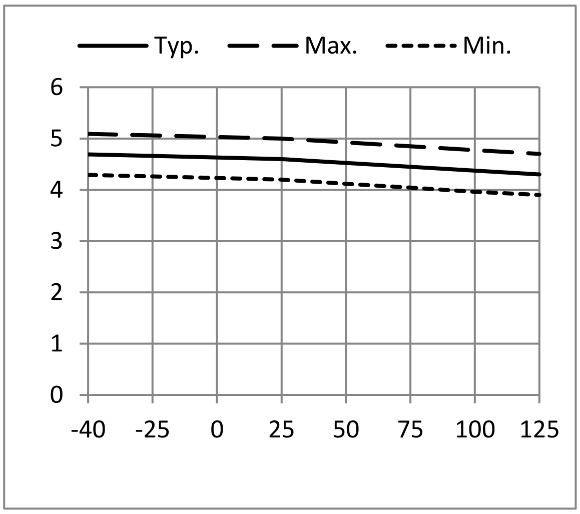


Figure 6A V_{BS} UVLO Threshold Voltage vs Temperature

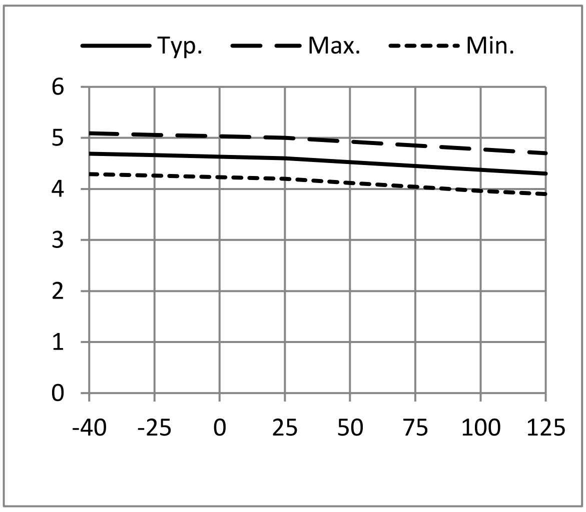


Figure 6B V_{BS} UVLO Reset Voltage vs Temperature

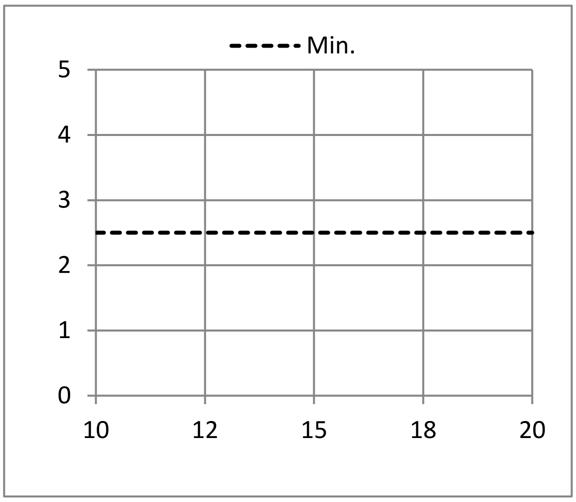


Figure 7A High-level Input Threshold Voltage vs Supply Voltage

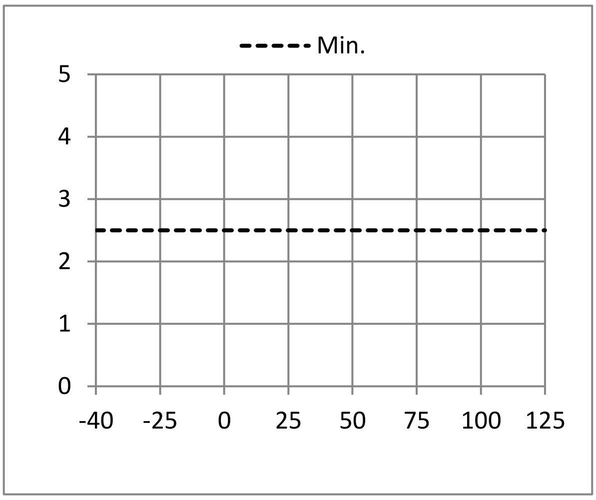


Figure 7B High-level Input Threshold Voltage vs Temperature

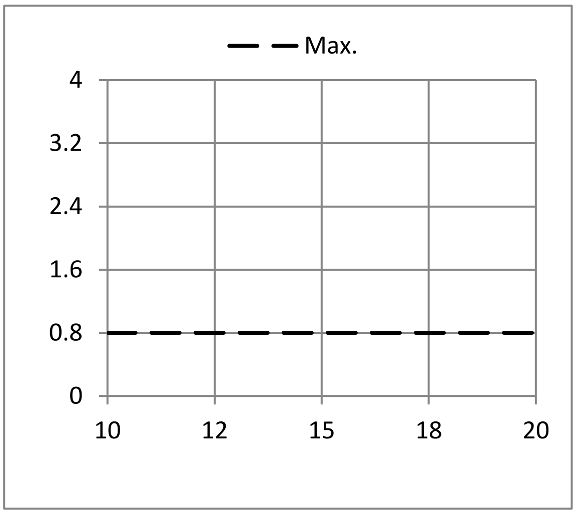


Figure 8A Low-level Input Threshold Voltage vs Supply Voltage

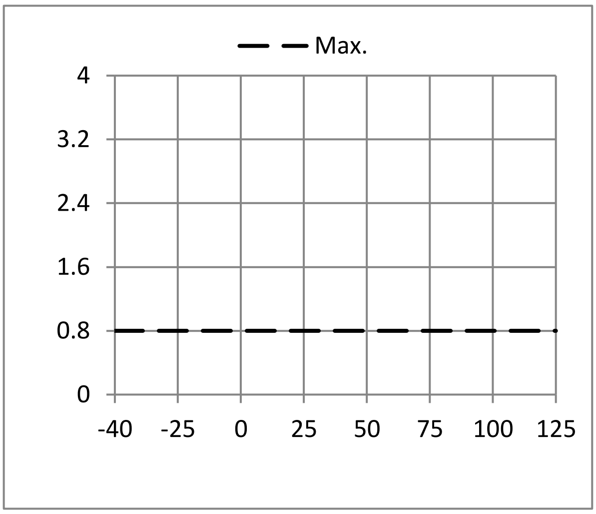


Figure 8B Low-level Input Threshold Voltage vs Temperature

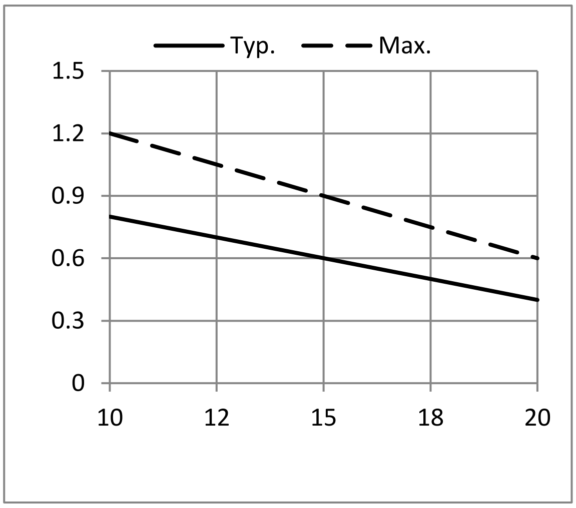


Figure 9A High-level Output Voltage vs Supply Voltage

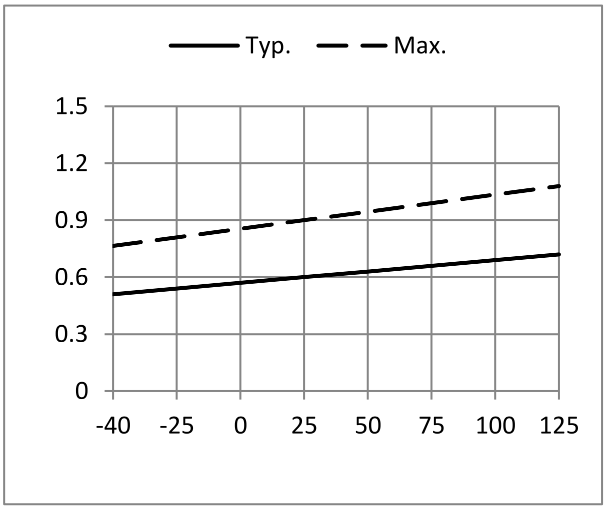


Figure 9B High-level Output Voltage vs Temperature

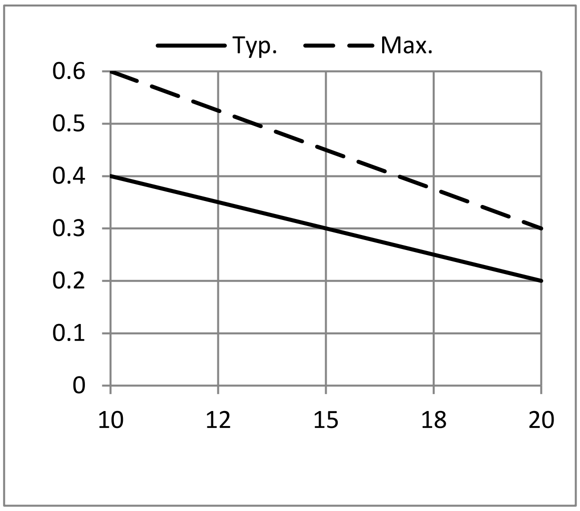


Figure 10A Low-level Output Voltage vs Supply Voltage

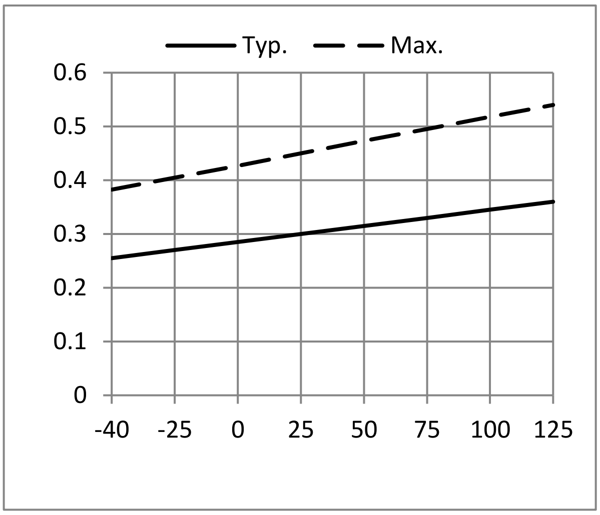


Figure 10B Low-level Output Voltage vs Temperature

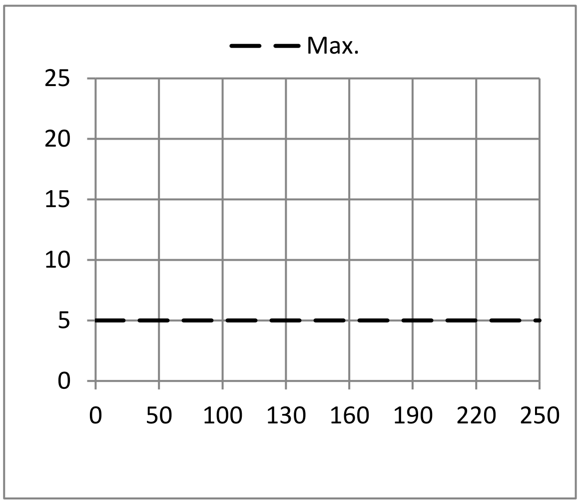


Figure 11A Leakage Current vs Supply Voltage

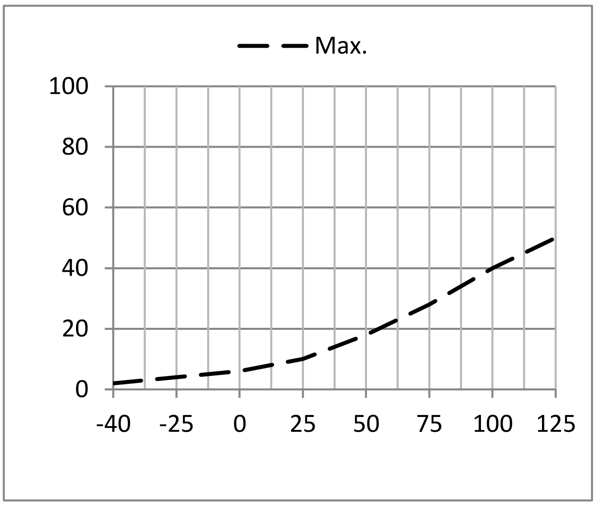


Figure 11B Leakage Current vs Temperature

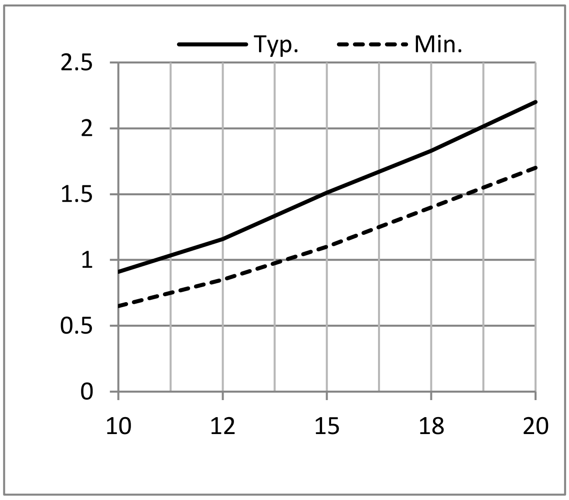


Figure 12A High-level Output Short-circuit

Pulse Current vs Supply Voltage

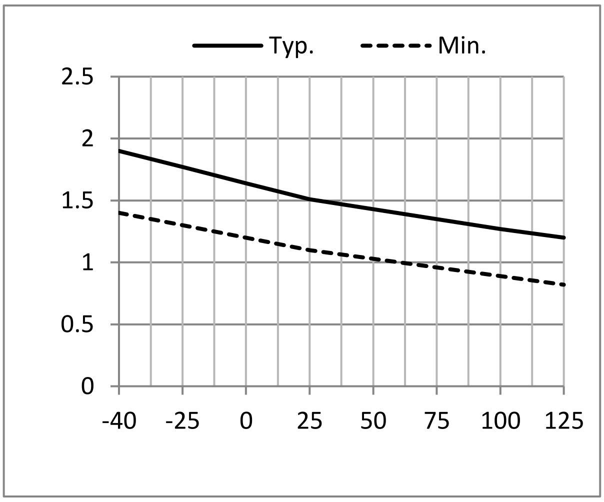


Figure 12B High-level Output Short-circuit

Pulse Current vs Temperature

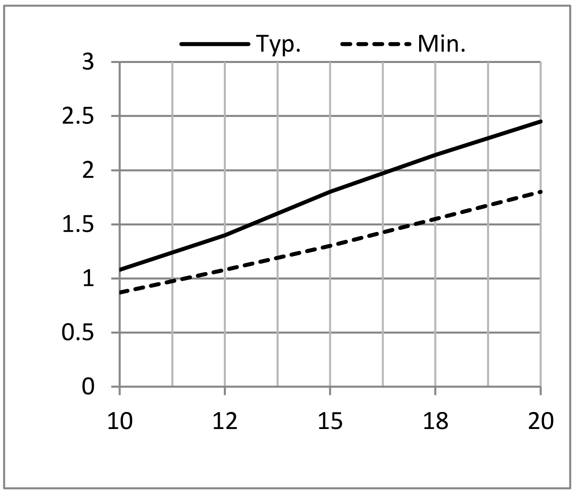


Figure 13A Low-level Output Short-circuit

Pulse Current vs Supply Voltage

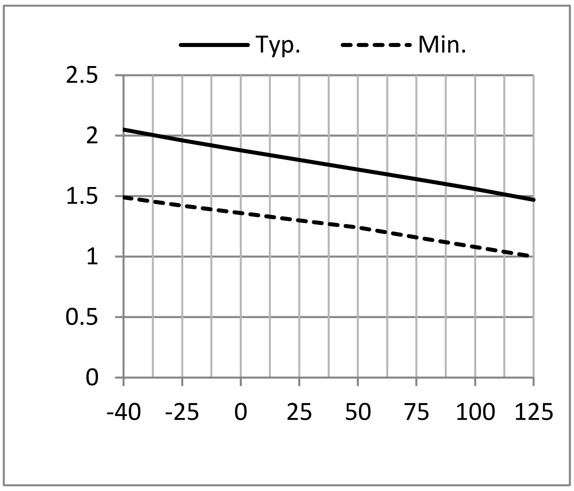


Figure 13B Low-level Output Short-circuit

Pulse Current vs Temperature

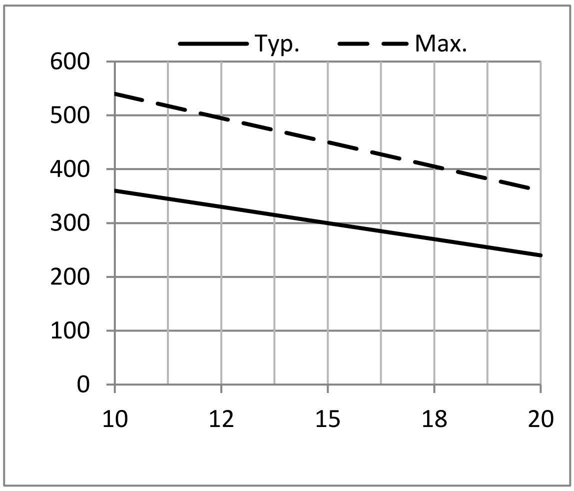


Figure 14A Turn-on Propagation Delay vs Supply Voltage

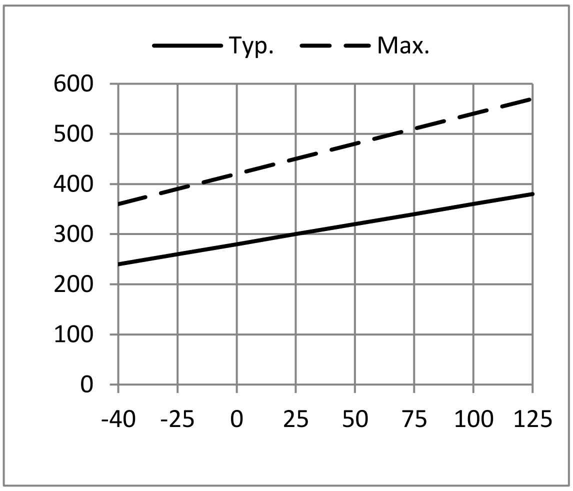


Figure 14B Turn-on Propagation Delay vs Temperature

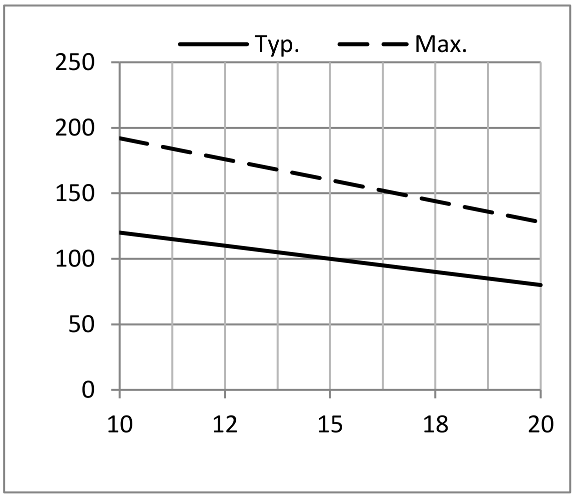


Figure 15A Turn-off Propagation Delay vs Supply Voltage

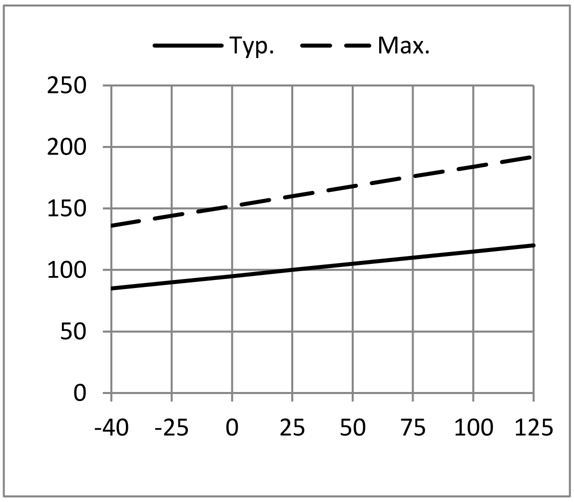


Figure 15B Turn-off Propagation Delay vs Temperature

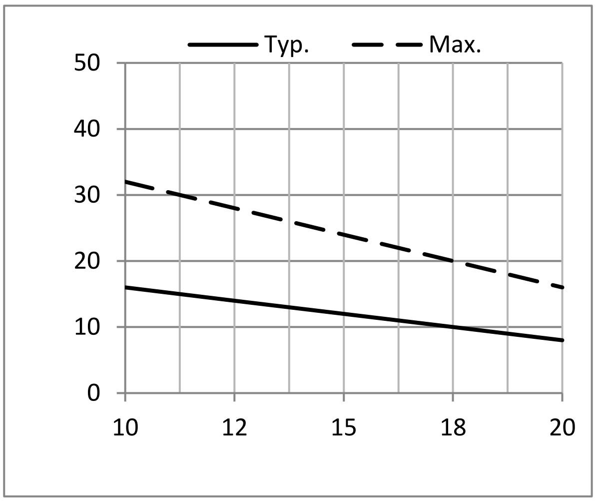


Figure16A Turn-on Rise Time vs Supply Voltage

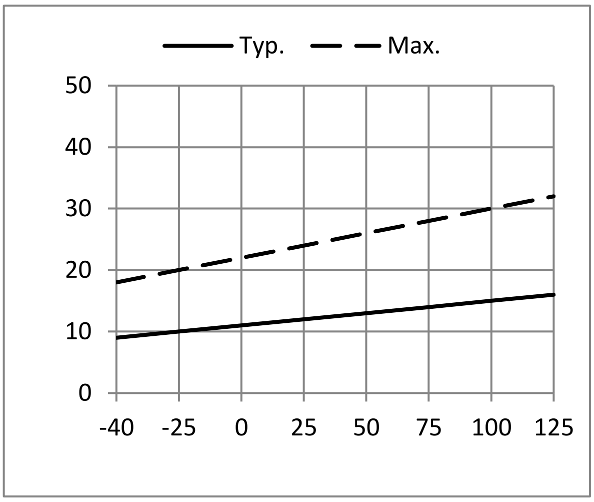


Figure 16B Turn-on Rise Time vs Temperature

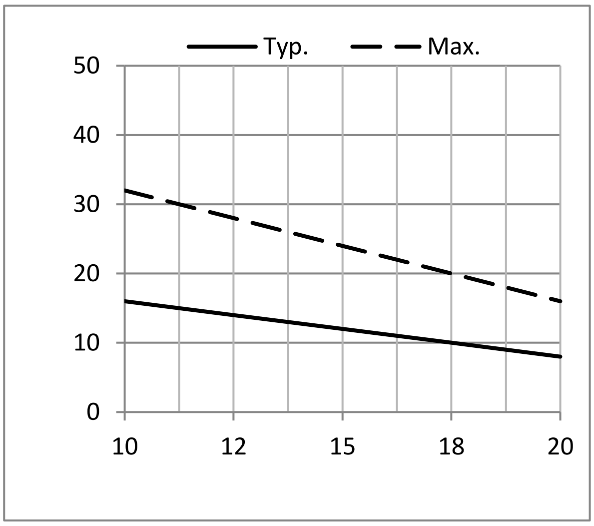


Figure 17A Turn-off Fall Time vs Supply Voltage

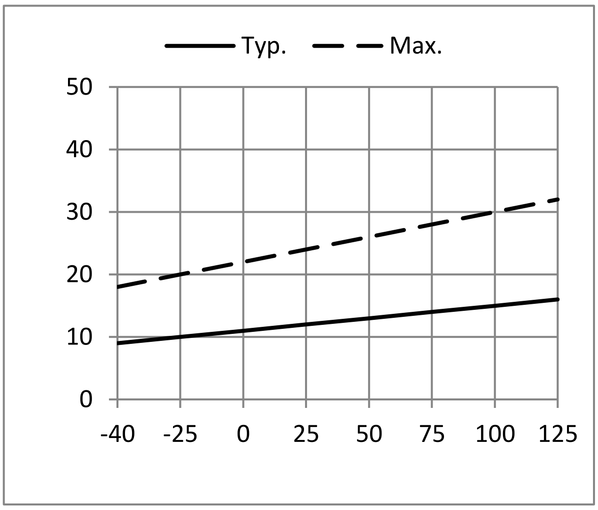


Figure 17B Turn-off Fall Time vs Temperature

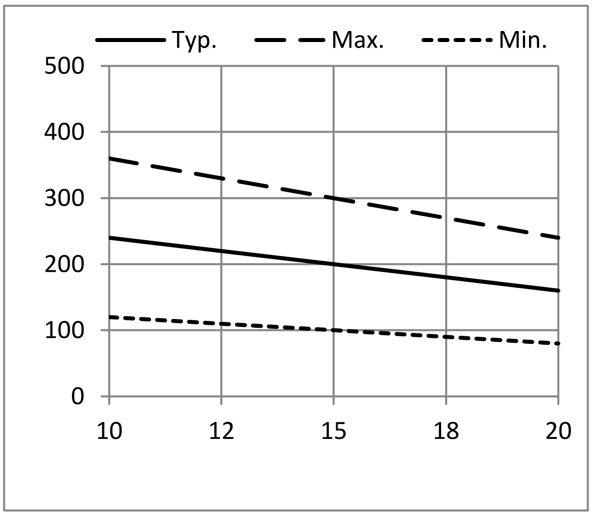


Figure 18A Deadtime vs Supply Voltage

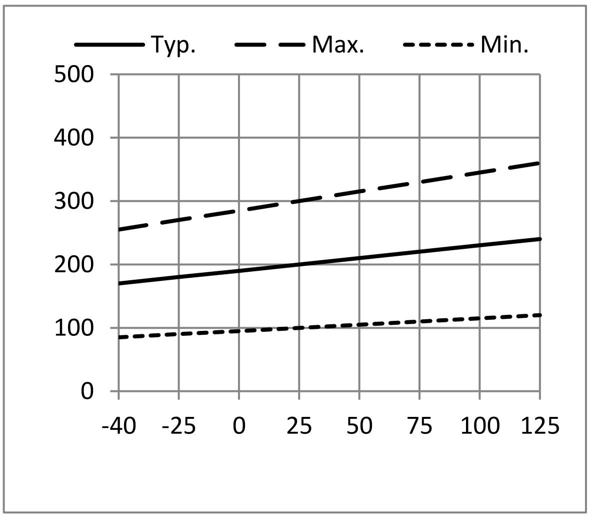


Figure 18B Deadtime vs Temperature

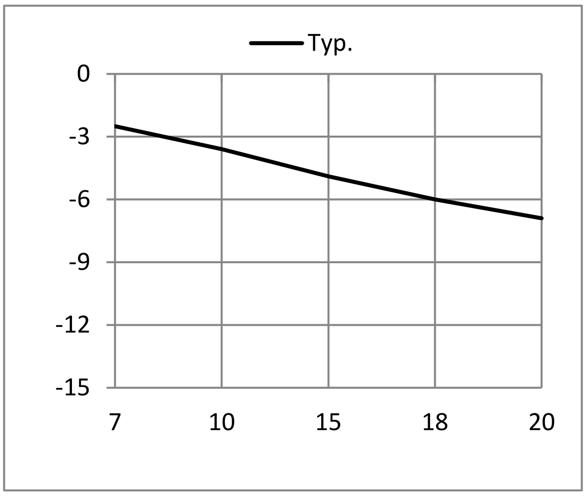


Figure 19A V_S Negative Offset vs Supply Voltage

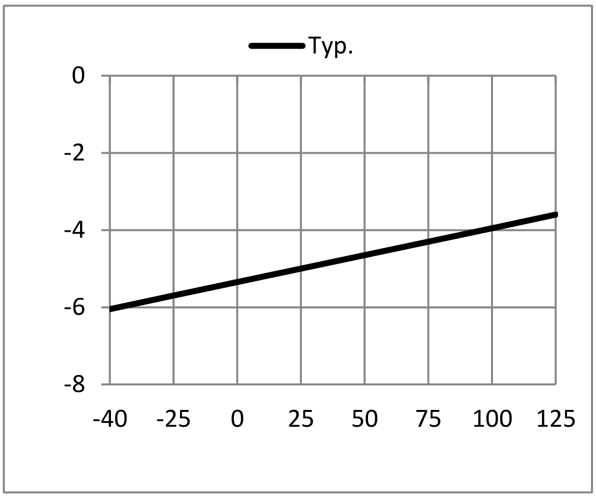


Figure 19B V_S Negative Offset vs Temperature

9 Revision History

Rev.	Descriptions	Date	Prepared By
V1.0	First release.	2016/04/18	Raymond Xie
V1.1	Added product model and changed ED6288 to ED6288T&Q.	2016/12/18	Raymond Xie
V1.2	Removed top-level silk prints and added packaging information.	2018/01/05	Raymond Xie
V1.3	Proofread some descriptions.	2019/01/22	Raymond Xie
V1.4	1. Added R2 resistor and related descriptions in Typical Application Diagram; 2. Corrected some descriptions and word spellings; 3. Standardized document format.	2023/04/24	Lay Ye / Eric Deng
V1.5	1. Proofread some descriptions in section 1 System Introduction; 2. Separated section Pin Diagrams and section Pin Definitions by ED6288T and ED6288Q; 3. Corrected some parameter names in section 3 Electrical Characteristics; 4. Added Cross-conduction Prevention and Deadtime.	2023/05/29	Eric Deng
V1.6	1. Updated section 1.6 Functional Block Diagram; 2. Modified chapter 2 Package Information; 3. Deleted "and it stays its logical state when $V_{S1,2,3}$ ranges from (COM-4V) to (COM-V_{BS})"in Note [3] of section 3.2 Recommended Operating Conditions; 4. Modified chip model ED6288T&Q as ED6288.	2023/09/01	Eric Deng

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