Datasheet

Half-bridge Gate Driver

ED2504S

Fortior Technology Co., Ltd.

Content

ED2504S Half-bridge Gate Driver

1 System Introduction

1.1 Overview

ED2504S is a high-voltage and high-speed gate driver that is used to drive N-channel power MOSFETs or IGBTs. It supports under-voltage lockout (UVLO) feature, protecting the power device from operating with insufficient voltage.

Its logic inputs are compatible with standard CMOS or LSTTL output (as low as 3.3V) and the output driver features a high pulse current buffer stage designed for minimum driver cross-conduction.

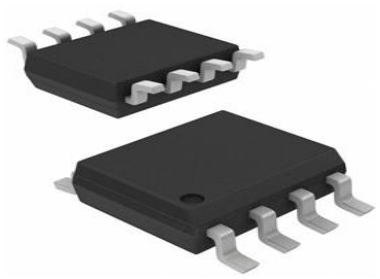
ED2504S also provides cross-conduction prevention and deadtime insertion to effectively protect the power device and prevent both MOSFETs or IGBTs of each half-bridge from switching on at the same time.

ED2504S can simultaneously turn off outputs from high and low channels.

1.2 Features

- Fully operational to +600V
- Output current: +0.29A/-0.6A
- 3.3V, 5V and 15V logic input compatible
- Under-voltage lockout (UVLO)
- High-side output in phase with input; Low-side output out of phase with the input
- Cross-conduction prevention logic
- Deadtime
- Turn off outputs from high and low channels
- Built-in V_{CC}/V_{BS} clamping circuit

1.3 Package



SOIC-8

1.4 Applications

- Motor drivers
- DC-DC converters
- DC-AC inverters
- Class-D power amplifiers

1.5 Typical Application Diagram

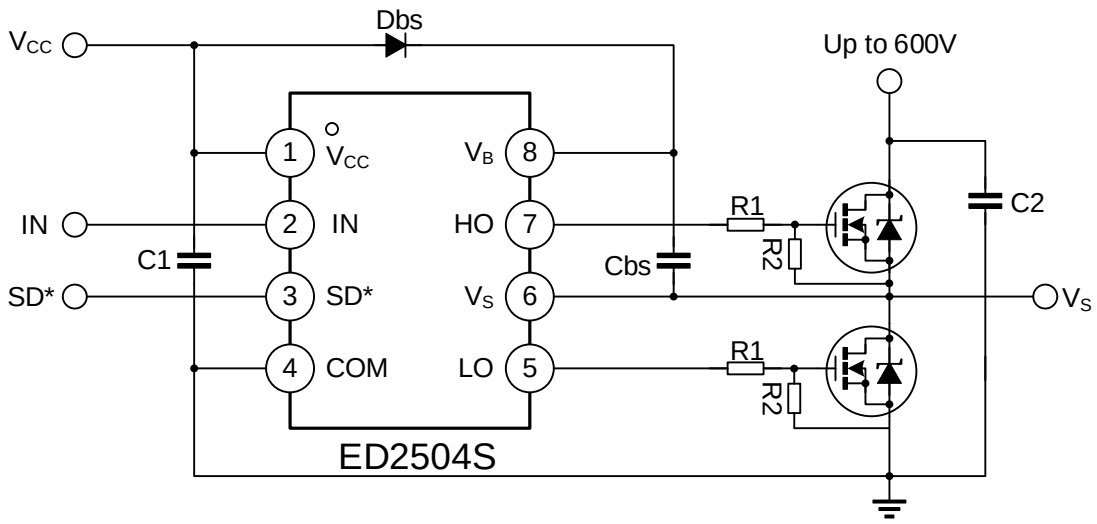


Figure 1-1 Typical Application Diagram of ED2504S

C1: Power filter capacitor; 10μF optional; as close to the chip pin as possible.

C2: High-voltage power filter capacitor. The capacitance depends on the application of circuit.

R1: Gate drive resistor. The resistance depends on the device being driven. 33 ~100Ω is recommended.

R2: MOS gate and source resistor. 10k~33kΩ is recommended.

D_{bs}: Bootstrap diodes. Those with high reverse breakdown voltage (>600V) and short recovery time are preferred.

C_{bs}: Bootstrap capacitors. Ceramic capacitors or tantalum capacitors are preferred. The minimum capacitance is calculated as follows:

$$C_{bs} \geq 15 \cdot \frac{2 \cdot [2 \cdot Q_g + Q_{period} + \frac{I_{bs(staic)}}{f} + \frac{I_{bs(leak)}}{f}]}{Vcc - V_F - V_{ds(L)}}$$

Where Q_g is the gate charge of high-side power device;

Q_{period} is the gate charge required by level-switching circuit in each cycle, which is about 10nC;

$I_{bs(staic)}$ is the static current of the high-side drive circuit;

$I_{bs(leak)}$ is the leakage current of the bootstrap capacitor;

F is the operating frequency of the circuit;

V_{CC} is the low-side supply voltage;

V_F is the forward turn-on voltage drop of the bootstrap diode;

$V_{ds(L)}$ is the turn-on voltage drop of the low-side power device.

Note: The above circuits and parameters are for reference only. The actual circuit shall be designed with the measured results.

1.6 Functional Block Diagram

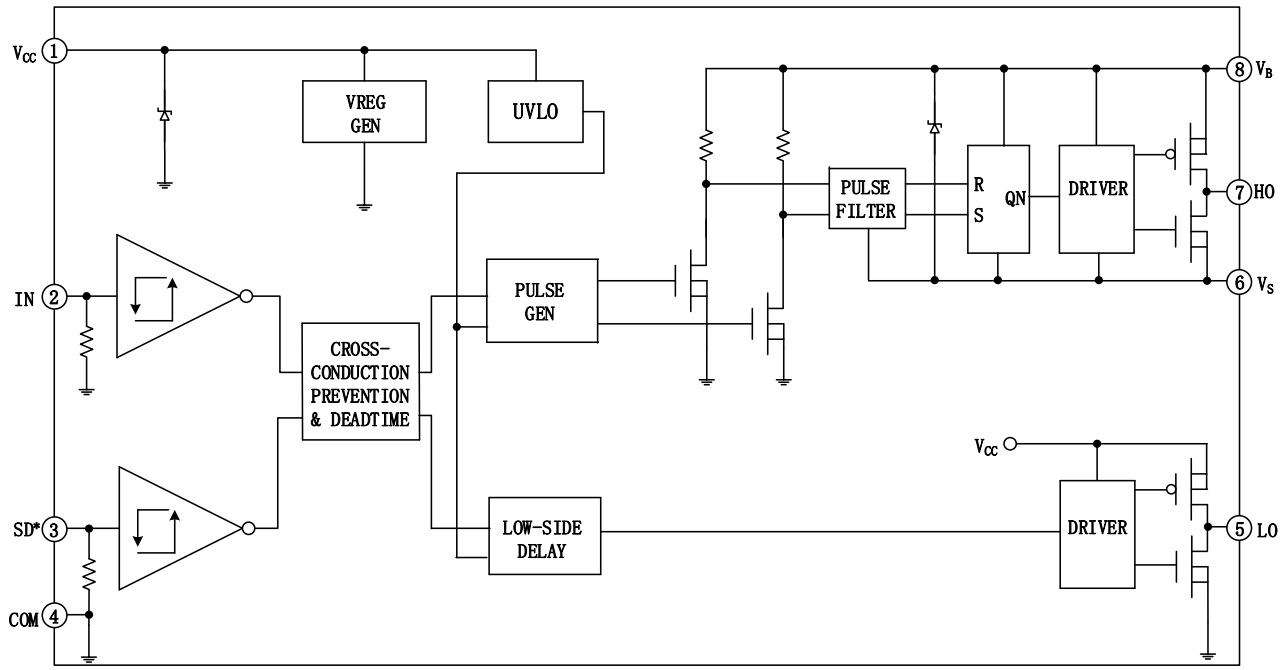


Figure 1-2 Functional Block Diagram of ED2504S

1.7 Pin Diagram

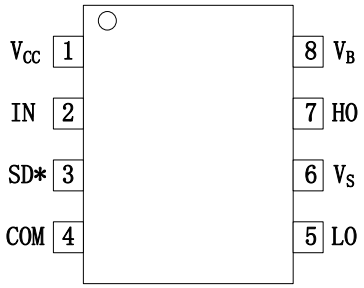


Figure 1-3 Pin Diagram of ED2504S

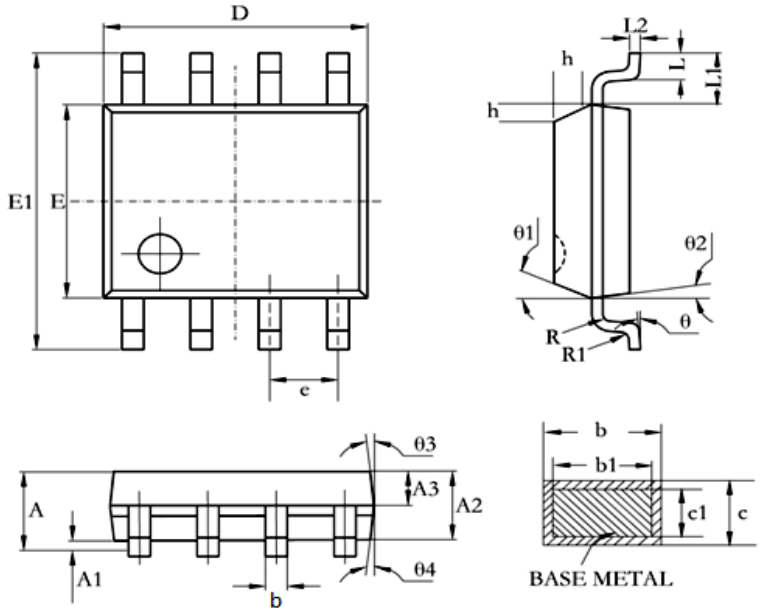
1.8 Pin Definitions

Table 1-1 ED2504S Pin Descriptions

Pin	Name	Description
1	V_{CC}	Low-side Power Supply
2	IN	Logic Input
3	SD*	Shutdown Inputs for High and Low Channels
4	COM	Ground
5	LO	Low-side Output
6	V_S	High-side Floating Offset Voltage
7	HO	High-side Output
8	V_B	High-side Floating Absolute Voltage

2 Package Information

2.1 ED2504S SOIC-8



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.36	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.25	1.40	1.65	0.049	0.055	0.065
A3	0.50	0.60	0.70	0.020	0.024	0.028
b	0.38	-	0.51	0.015	-	0.020
b1	0.37	0.42	0.47	0.015	0.017	0.019
c	0.17	-	0.25	0.007	-	0.010
c1	0.17	0.20	0.23	0.007	0.008	0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	5.80	6.00	6.20	0.228	0.236	0.244
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC					
L	0.45	0.60	0.80	0.018	0.024	0.031
L1	1.04REF					
L2	0.25BSC					
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
h	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	-	8°	0°	-	8°
θ1	15°	17°	19°	15°	17°	19°
θ2	11°	13°	15°	11°	13°	15°
θ3	15°	17°	19°	15°	17°	19°
θ4	11°	13°	15°	11°	13°	15°

Product Number	Package Type	Marking ID	Package Method	Quantity
ED2504S	SOP8	ED2504S	Tape & Reel	2500

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

(All pins are referenced to COM unless otherwise specified.)

Parameter	Symbol	Min. ~ Max.	Unit
High-side Floating Absolute Voltage	V_B	-0.3～625	V
High-side Floating Offset Voltage	V_S	V_B-25～V_B+0.3	V
High-side Output Voltage	V_{HO}	V_S-0.3～V_B+0.3	V
Low-side Power Supply	V_{CC}	-0.3～25	V
Low-side Output Voltage	V_{LO}	-0.5～V_{CC}+0.3	V
Logic Input Voltage (IN, SD*)	V_{IN}	-0.5～V_{CC}+0.3	V
Swing Rate of Offset Voltage	dV_S/dt	≤50	V/ns
Power Dissipation @T_A≤25°C	P_D	≤0.625	W
Junction-to-Ambient Thermal Resistance	R_{thJA}	≤200	°C/W
Junction Temperature	T_j	≤150	°C
Storage Temperature	T_{stg}	-55～150	°C

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

(All voltages are referenced to COM unless otherwise specified.)

Parameter	Symbol	Min.	Max.	Unit
High-side Floating Absolute Voltage	V_B	V_S+10	V_S+20	V
High-side Floating Offset Voltage	V_S	-7	600	V
High-side Output Voltage	V_{HO}	V_S	V_B	V
Low-side Power Supply	V_{CC}	10	20	V
Low-side Output Voltage	V_{LO}	0	V_{CC}	V
Logic Input Voltage (IN, SD*)	V_{IN}	0	V_{CC}	V
Ambient Temperature	T_A	-40	125	°C

3.3 Static Electrical Characteristics

Table 3-3 Static Electrical Characteristics

[T_A =25°C, V_{BIAS} (V_{CC}, V_{BS}) =15V and V_S=COM unless otherwise specified.]

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Threshold Voltage	V_{IH}	V_{CC} = 10V to 20V	2.5	-	-	V
Low-level Input Threshold Voltage	V_{IL}		-	-	0.8	
SD* High-level Input Threshold Voltage	$V_{SD*,TH+}$		2.5	-	-	
SD* Low-level Input Threshold Voltage	$V_{SD*,TH-}$		-	-	0.8	

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-level Output Voltage V_{BIAS} - V_O	V_{OH}	I_O = 2mA	-	0.05	0.2	
Low-level Output Voltage V_O	V_{OL}		-	0.02	0.1	
Leakage Current of Floating Power Supply	I_{LK}	$V_B = V_S$ = 600V	-	-	10	uA
V_{BS} Quiescent Current	I_{QBS}	V_{IN} = 0V or 5V	-	22	50	
V_{CC} Quiescent Current	I_{QCC}		-	105	200	
High-level Input Bias Current	I_{IN+}	V_{IN} = 5V	-	20	40	
Low-level Input Bias Current	I_{IN-}	V_{IN} = 0V	-	-	1	
V_{CC} UVLO Threshold Voltage	V_{CCUV+}		8.1	9	9.9	V
V_{CC} UVLO Reset Voltage	V_{CCUV-}		7.5	8.3	9.1	
V_{CC} UVLO Hysteresis Voltage	V_{CCUVH}		0.3	0.7	-	
High-level Output Short-circuit Pulse Current	I_{O+}	V_O=0V; PW≤10us	150	290	-	mA
Low-level Output Short-circuit Pulse Current	I_{O-}	V_O=15V; PW≤10us	300	600	-	

3.4 Dynamic Electrical Characteristics

Table 3-4 Dynamic Electrical Characteristics

[T_A =25°C, V_{BIAS} (V_{CC}, V_{BS}) =15V, C_L=1000pF and V_S=COM unless otherwise specified.]

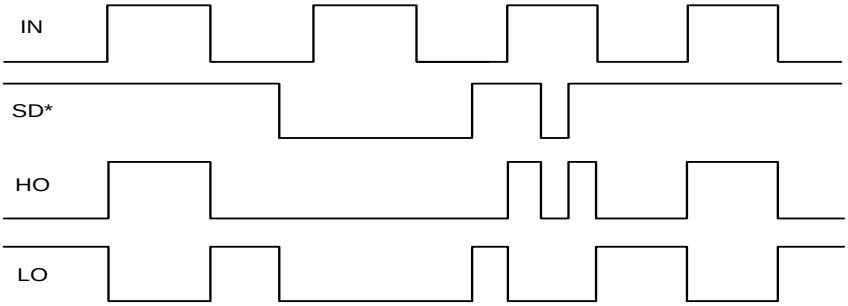
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Propagation Delay	t_{on}	V_S=0V	-	660	820	ns
Turn-off Propagation Delay	t_{off}	V_S=600V	-	150	220	
High-low Side Delay Match	MT		-	0	60	
SD* Shutdown Propagation Delay	t_{sd}		-	160	220	
Turn-on Rise Time	t_r		-	70	140	
Turn-off Fall Time	t_f		-	35	70	
Deadtime	DT		400	520	650	

3.5 Logic Function List

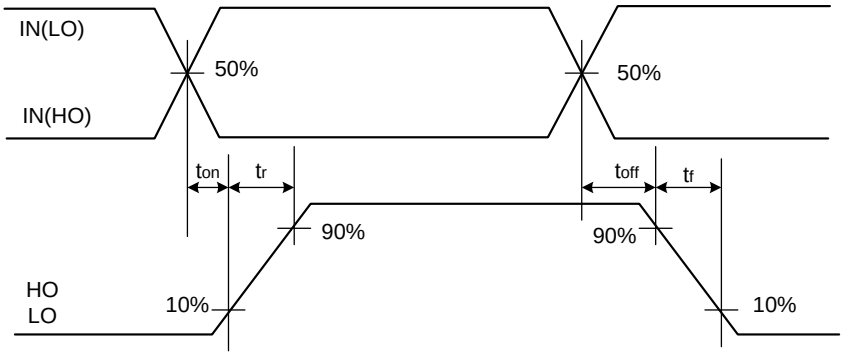
IN	SD*	V_{CC} UV	HO	LO
L	H	H	L	H
H	H	H	H	L
X	L	H	L	L
X	X	L	L	L

Note: V_{CC} UV is lower than V_{CC} UVLO detection voltage when it is “L”.

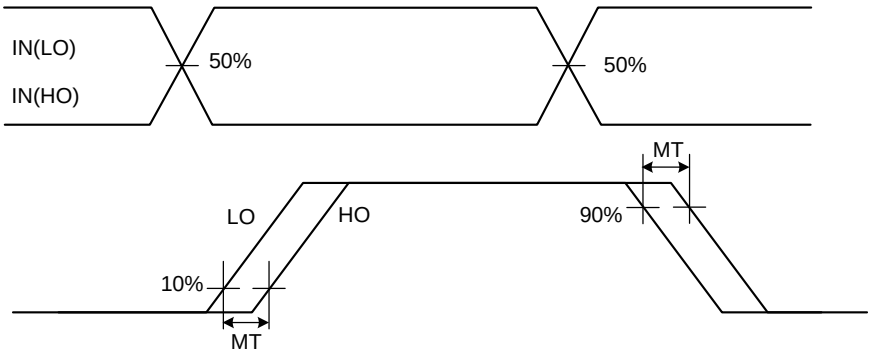
4 Logic Function Timing Diagram



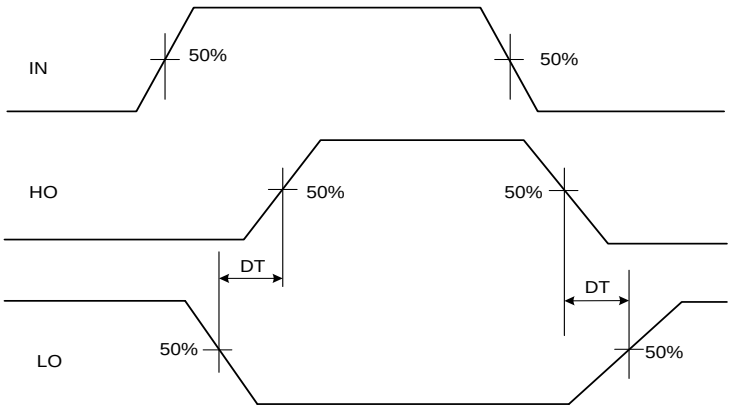
5 Propagation Delay Waveform Definitions



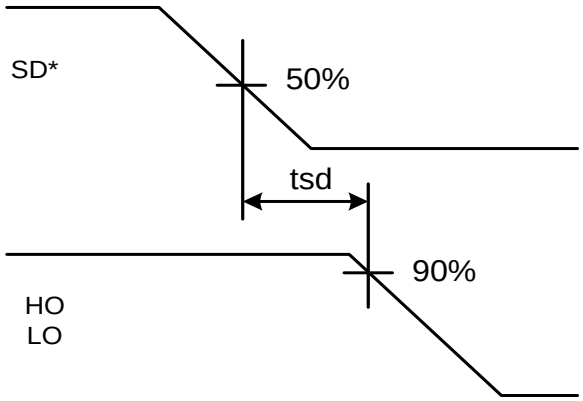
6 Propagation Delay Matching Waveform Definitions



7 Deadtime Waveform Definitions



8 Shutdown Waveform Definitions



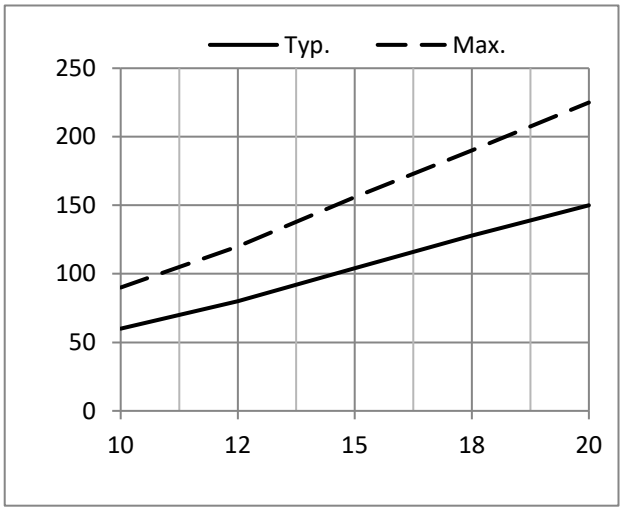


Figure 1A V_{CC} Supply Current vs V_{CC} Supply Voltage

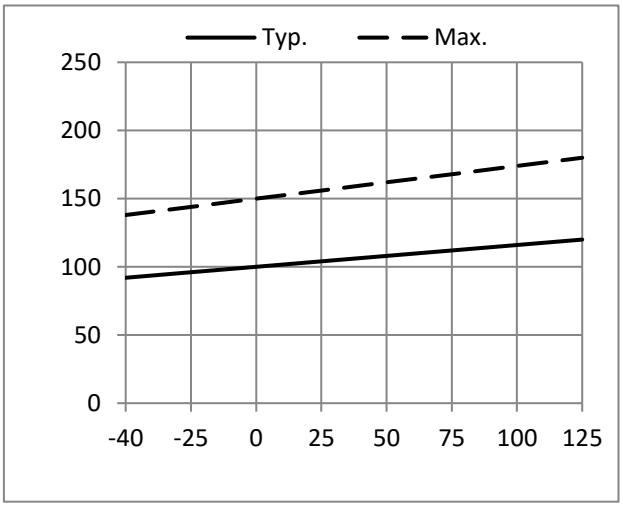


Figure 1B V_{CC} Supply Current vs Temperature

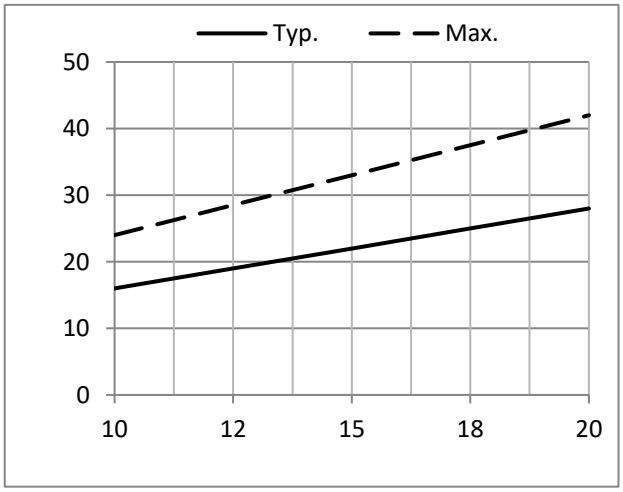


Figure 2A V_{BS} Supply Current vs V_{BS} Supply Voltage

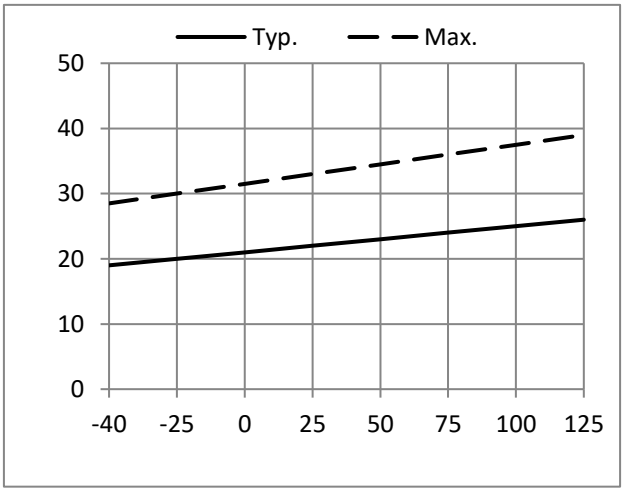


Figure 2B V_{BS} Supply Current vs Temperature

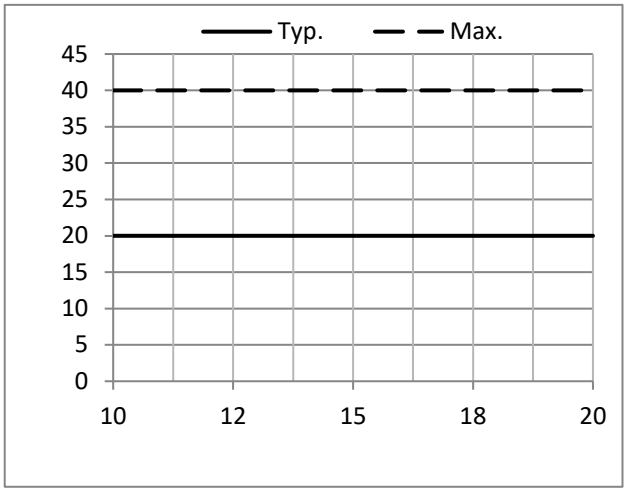


Figure 3A High-level Input Bias Current vs V_{CC} Supply Voltage

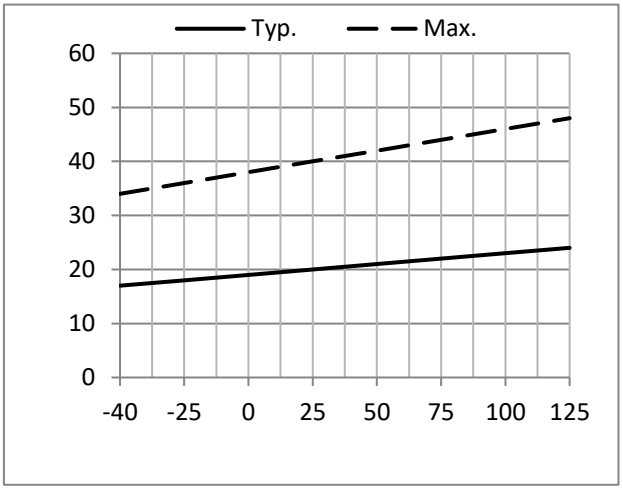


Figure 3B High-level Input Bias Current vs Temperature

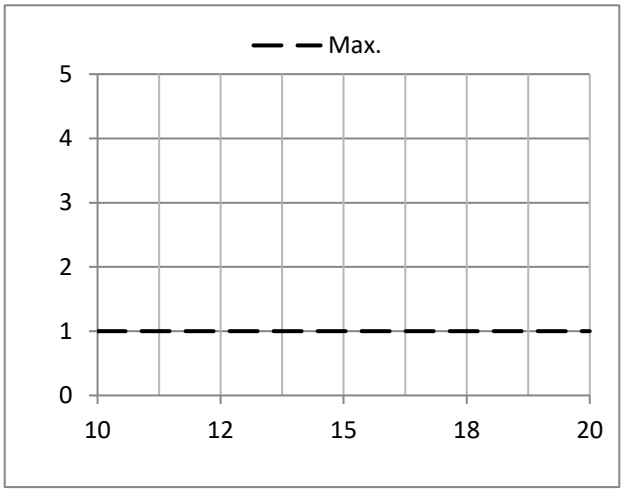


Figure 4A Low-level Input Bias Current vs V_{CC} Supply Voltage

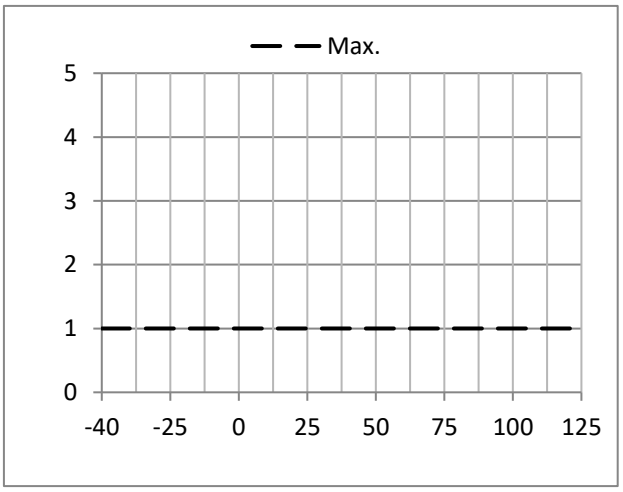


Figure 4B Low-level Input Bias Current vs Temperature

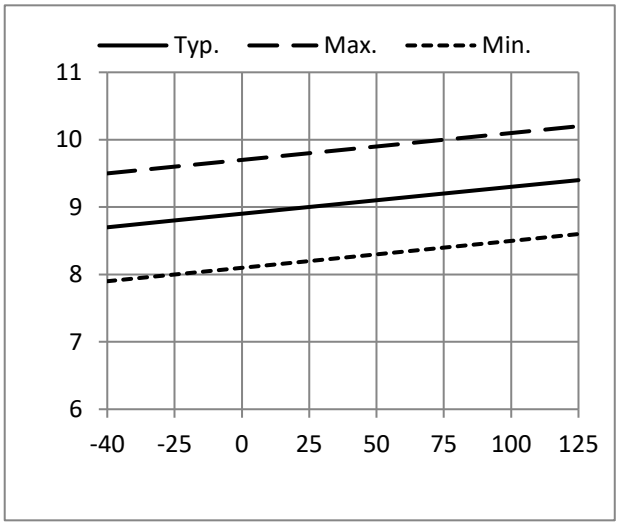


Figure 5A V_{CC} UVLO Threshold Voltage vs Temperature

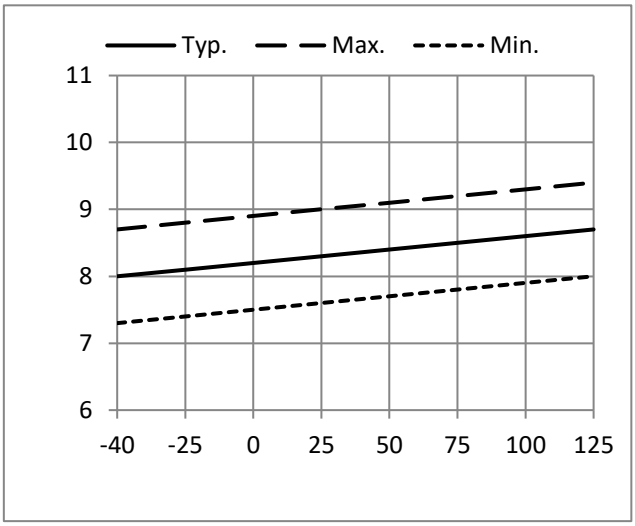


Figure 5B V_{CC} UVLO Reset Voltage vs Temperature

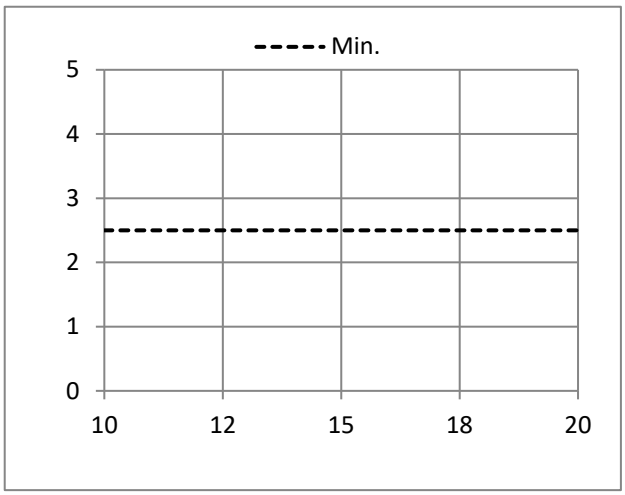


Figure 6A High-level Input Threshold Voltage vs V_{CC} Supply Voltage

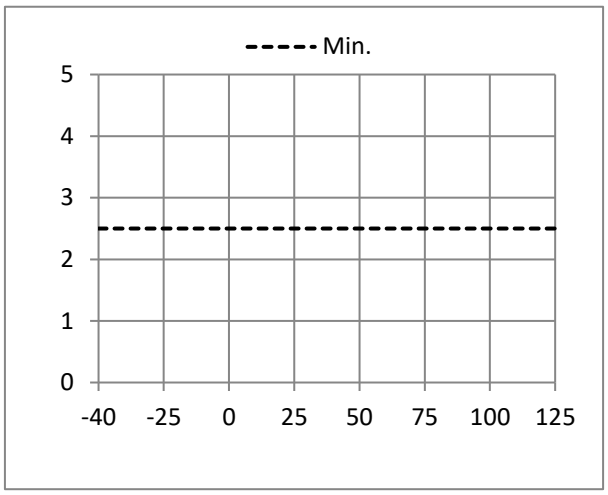


Figure 6B High-level Input Threshold Voltage vs Temperature

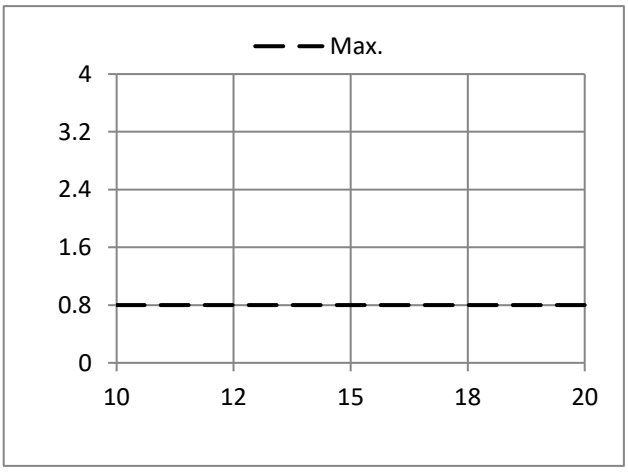


Figure 7A Low-level Input Threshold Voltage vs V_{CC} Supply Voltage

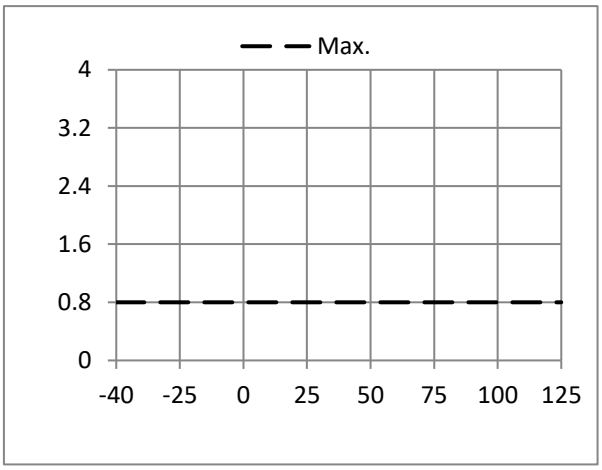


Figure 7B Low-level Input Threshold Voltage vs Temperature

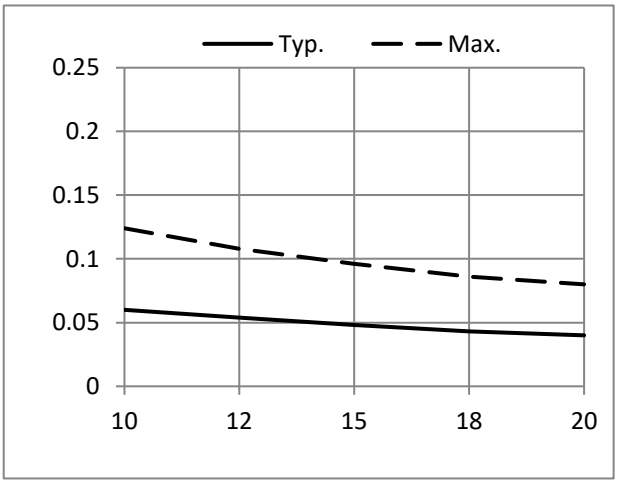


Figure 8A High-level Output Voltage vs Supply Voltage

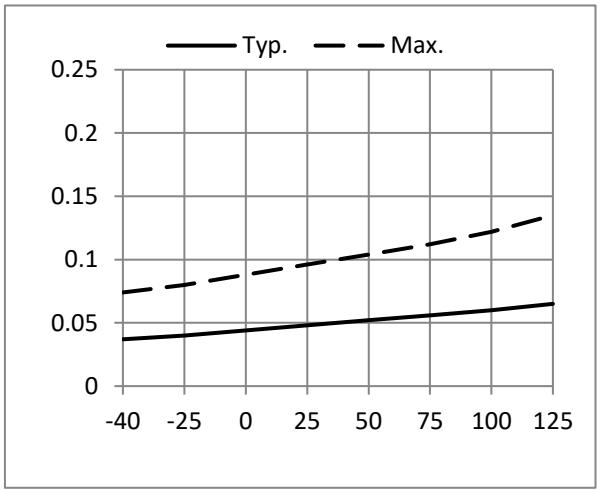


Figure 8B High-level Output Voltage vs Temperature

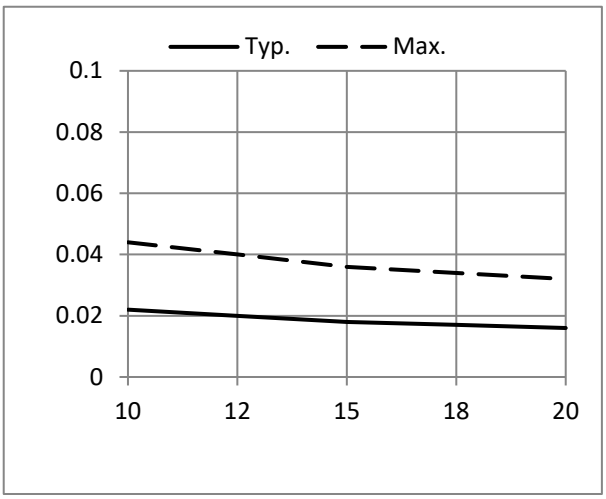


Figure 9A Low-level Output Voltage vs Supply Voltage

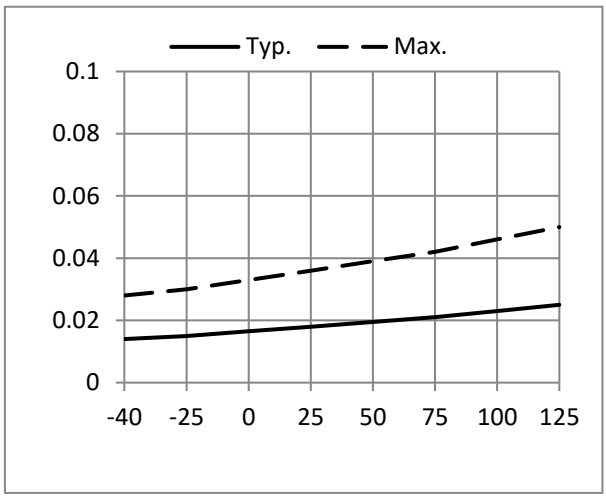


Figure 9B Low-level Output Voltage vs Temperature

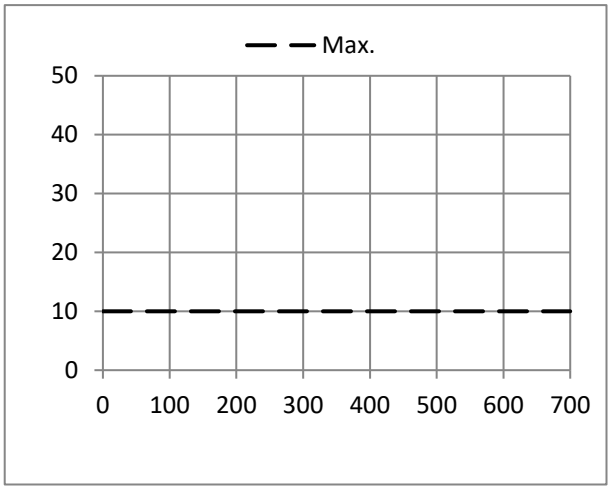


Figure 10A Leakage Current vs V_B Voltage

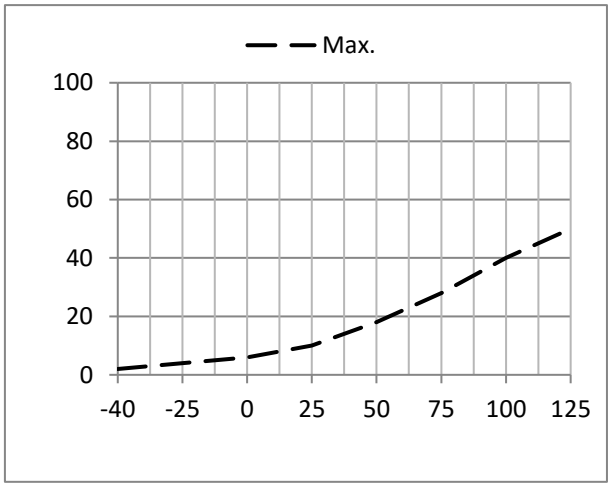


Figure 10B Leakage Current vs Temperature

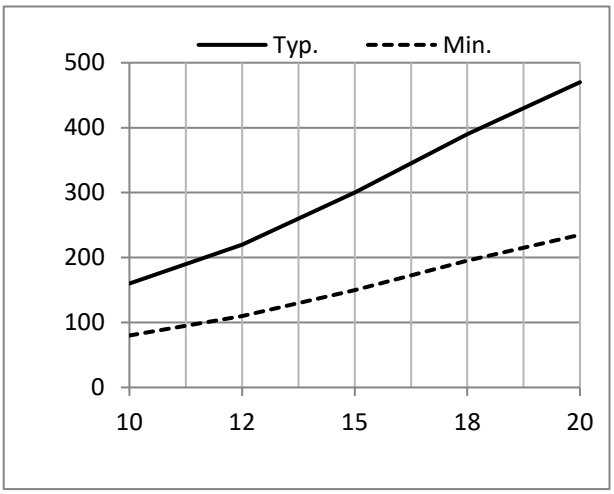


Figure 11A High-level Output Short-circuit

Pulse Current vs Supply Voltage

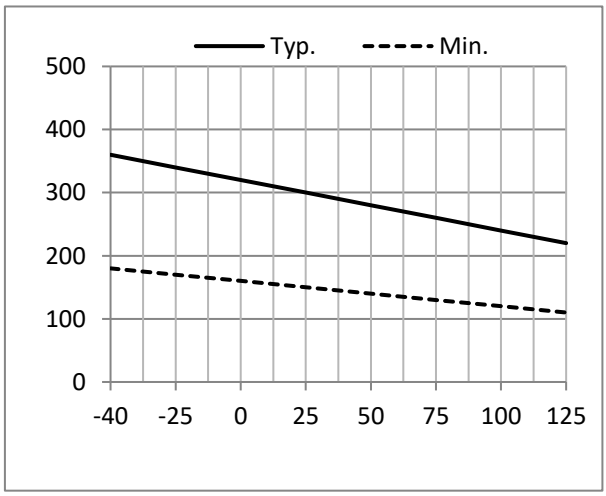


Figure 11B High-level Output Short-circuit

Pulse Current vs Temperature

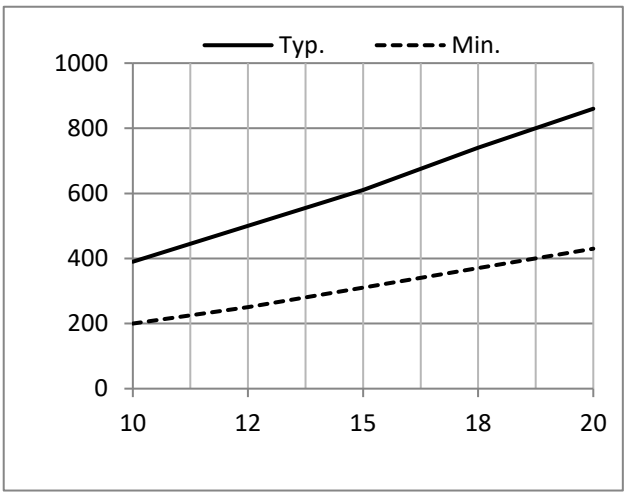


Figure 12A Low-level Output Short-circuit Pulse Current vs Supply Voltage

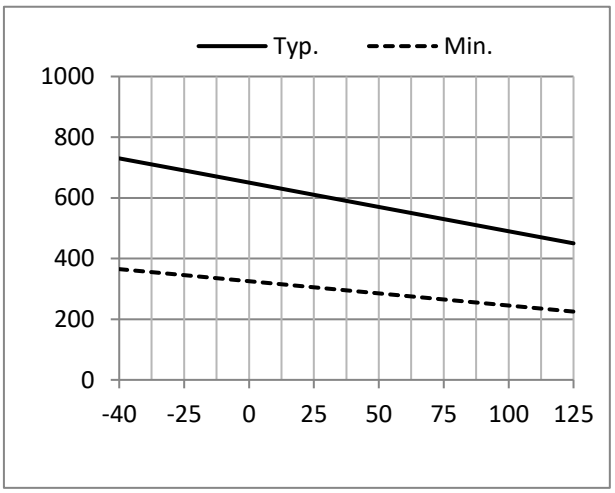


Figure 12B Low-level Output Short-circuit Pulse Current vs Temperature

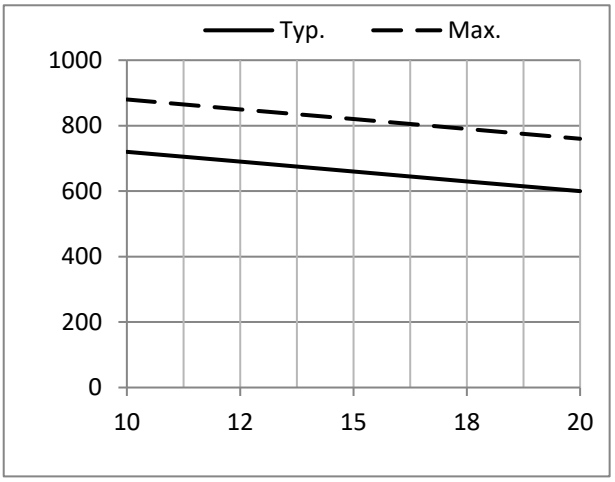


Figure 13A Turn-on Propagation Delay vs Supply Voltage

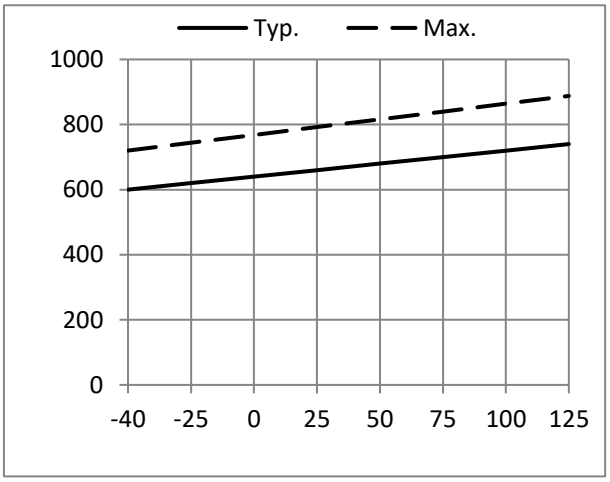


Figure 13B Turn-on Propagation Delay vs Temperature

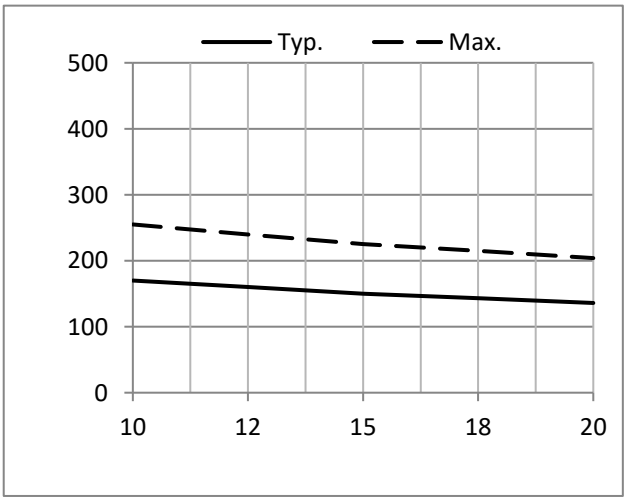


Figure 14A Turn-off Propagation Delay vs Supply Voltage

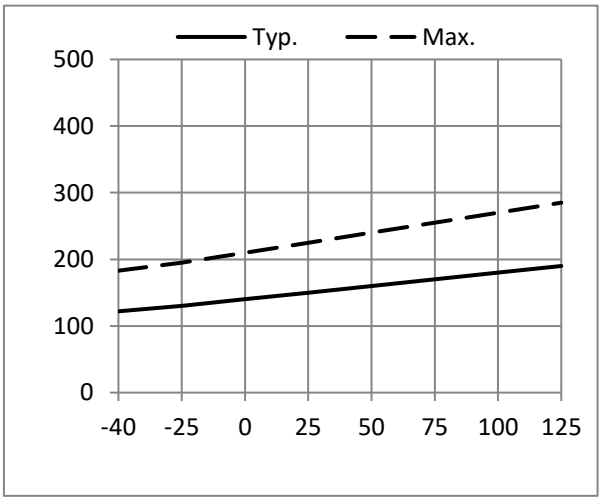


Figure 14B Turn-off Propagation Delay vs Temperature

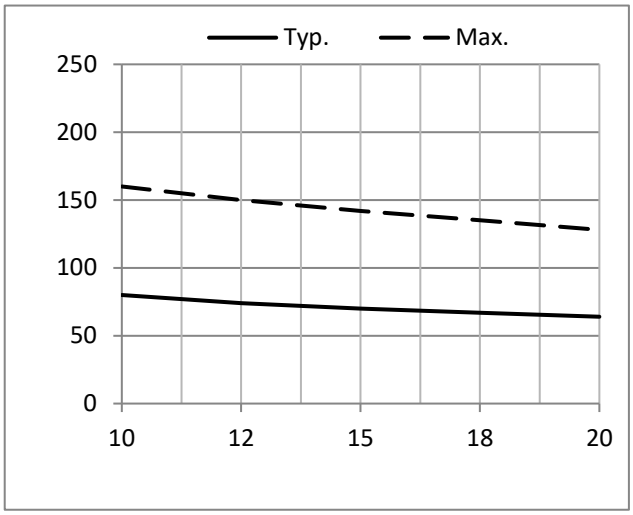


Figure15A Turn-on Rise Time vs Supply Voltage

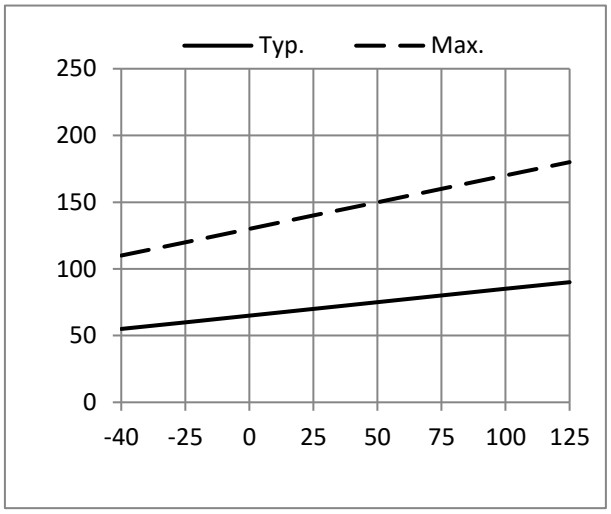


Figure 15B Turn-on Rise Time vs Temperature

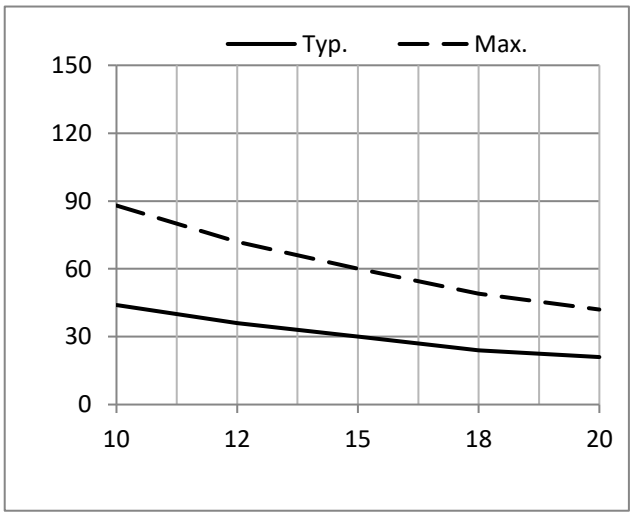


Figure 16A Turn-off Fall Time vs Supply Voltage

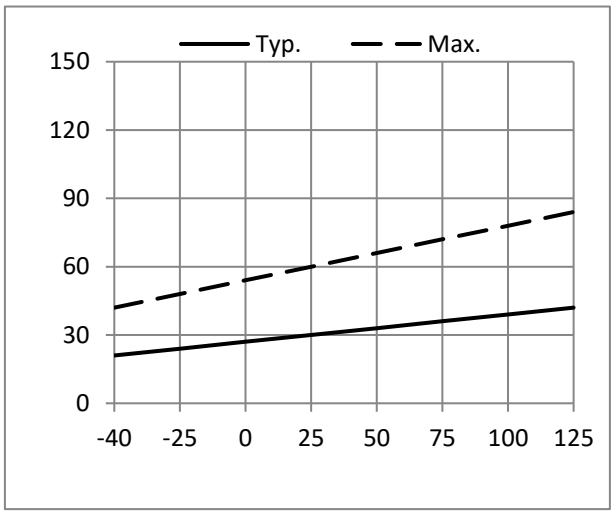


Figure 16B Turn-off Fall Time vs Temperature

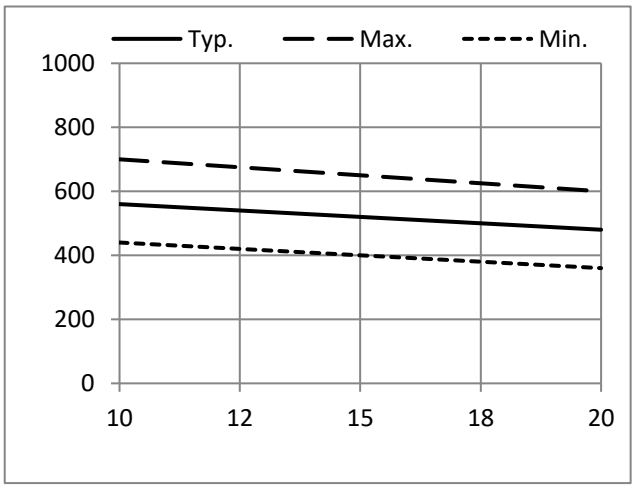


Figure 17A Deadtime vs Supply Voltage

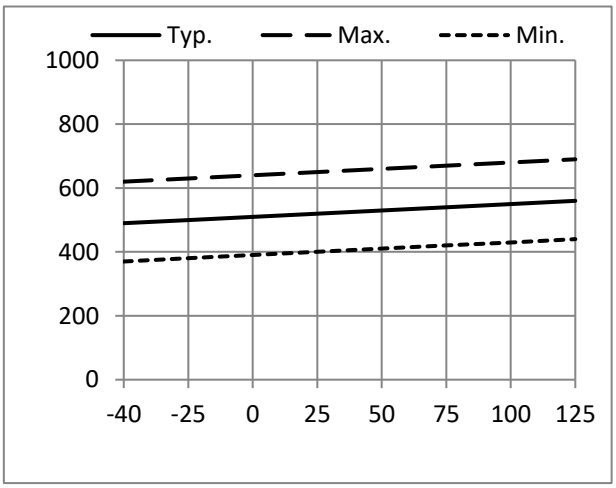


Figure 17B Deadtime vs Temperature

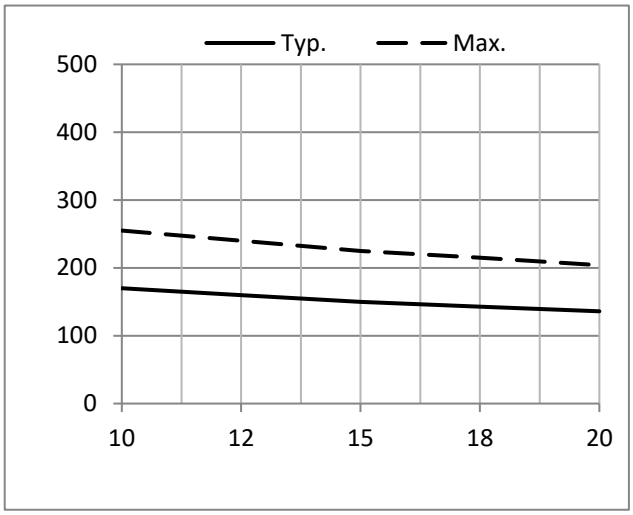


Figure 18A Shutdown Propagation Delay vs Supply Voltage

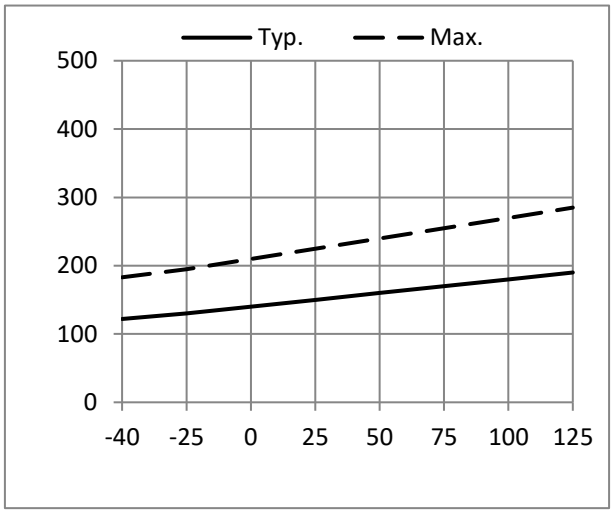


Figure 18B Shutdown Propagation Delay vs Temperature

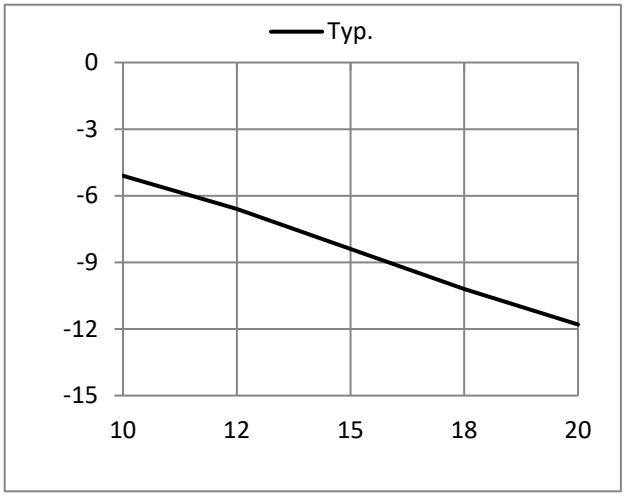


Figure 19A V_S Negative Offset vs Supply Voltage

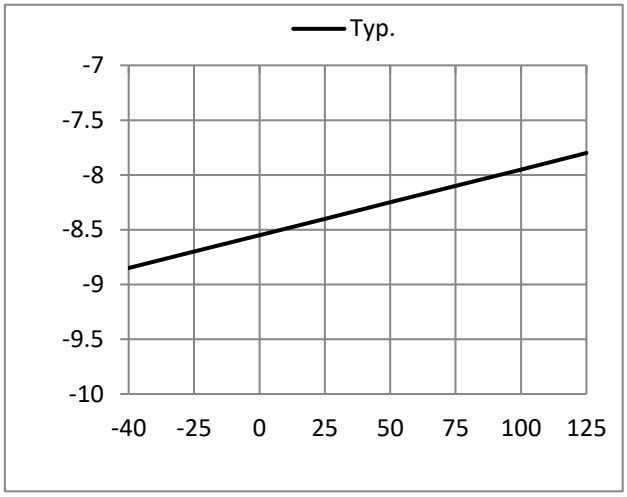


Figure 19B V_S Negative Offset vs Temperature

9 Revision History

Rev.	Descriptions	Date	Prepared By
V1.0	First release.	2014/09/23	Raymond Xie
V1.1	Corrected a letter “d” in the figure of section Case Outlines as “b”.	2015/08/18	Mingxian Jiang
V1.2	Modified the Product Number ED2504S as ED2504S.	2016/12/18	Raymond Xie
V1.3	1. Deleted the section Park Marking Information; 2. Added Marking ID and Quantity in section Package Information.	2023/05/22	Raymond Xie
V1.4	1. Added R2 resistor and detailed descriptions in section 1.5 Typical Application Diagram; 2. Modified maximum value of high-side floating offset voltage in section 1.2 Features, Figure 1-1 Typical Application Diagram of ED2504S and Table 3-2 Recommended Operating Conditions from 650V to 600V; 3. Corrected some parameter names in section 3 Electrical Characteristics; 4. Proofread some descriptions in section 1 System Introduction and section 8 Shutdown Waveform Definitions; 5. Standardized the document format.	2023/05/22	Eric Deng

Copyright Notice

Right to make changes — Fortior Technology Co., Ltd. reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. The information contained in this manual is provided for the general use by our customers. Our customers should ensure that they take appropriate action so that their use of our products does not infringe upon any patents. It is the policy of Fortior Technology Co., Ltd. to respect the valid patent rights of third parties and not to infringe upon or assist others to infringe upon such rights.

If there are any differences between the Chinese and the English contents, please take the Chinese version as the standard.

Fortior Technology Co., Ltd.
(Singapore): 1003 Bukit Merah Central, #04-22, INNO Center, (s)159836
Customer service: info@fortiortech.com
URL: http://www.fortiortech.com/global/