

## Datasheet

**600V Half-bridge Gate Driver**

**ED2607S**

Fortior Technology Co., Ltd.

**Contents**

<b>1 System Introduction.....</b>	<b>3</b>
1.1 Overview .....	3
1.2 Package .....	3
1.3 Features .....	3
1.4 Applications.....	3
1.5 Typical Application Diagram.....	4
1.6 Functional Block Diagram .....	5
1.7 Pin Definitions.....	6
1.7.1 ED2607S Pin Diagram.....	6
1.7.2 ED2607S Pin Descriptions .....	6
<b>2 Package Information .....</b>	<b>7</b>
2.1 ED2607S SOP8.....	7
<b>3 Electrical Characteristics.....</b>	<b>8</b>
3.1 Absolute Maximum Ratings .....	8
3.2 Recommended Operating Conditions.....	8
3.3 Static Electrical Characteristics .....	9
3.4 Dynamic Electrical Characteristics .....	9
<b>4 Logic Function Timing Diagram .....</b>	<b>10</b>
<b>5 Propagation Delay Test Standards.....</b>	<b>10</b>
<b>6 Propagation Delay Matching Test Standards.....</b>	<b>10</b>
<b>7 Cross-conduction Prevention.....</b>	<b>11</b>
<b>8 Deadtime .....</b>	<b>11</b>
<b>9 Revision History.....</b>	<b>12</b>

## ED2607S 600V Half-bridge Gate Driver

### 1 System Introduction

#### 1.1 Overview

ED2607S is a high-voltage, high-speed and half-bridge gate driver that is used to drive N-type power MOSFETs and IGBTs.

ED2607S supports under-voltage lockout (UVLO) feature, protecting the power device from operating with insufficient voltage.

ED2607S provides cross-conduction prevention and deadtime insertion to effectively protect the power device and prevent both MOSFETs or IGBTs of each half-bridge from switching on at the same time.

#### 1.2 Package



#### 1.3 Features

- Fully operational to +600V
- Power supply: 10V ~20V
- 3.5V/5V input logic compatible
- V<sub>CC</sub> under-voltage lockout (UVLO)
- Output in phase with the input
- Cross-conduction prevention logic
- Deadtime
- Matched propagation delay for high-side and low-side channels
- RoHS compliant

#### 1.4 Applications

- Motor drivers
- DC-DC converters
- DC-AC inverters

## 1.5 Typical Application Diagram

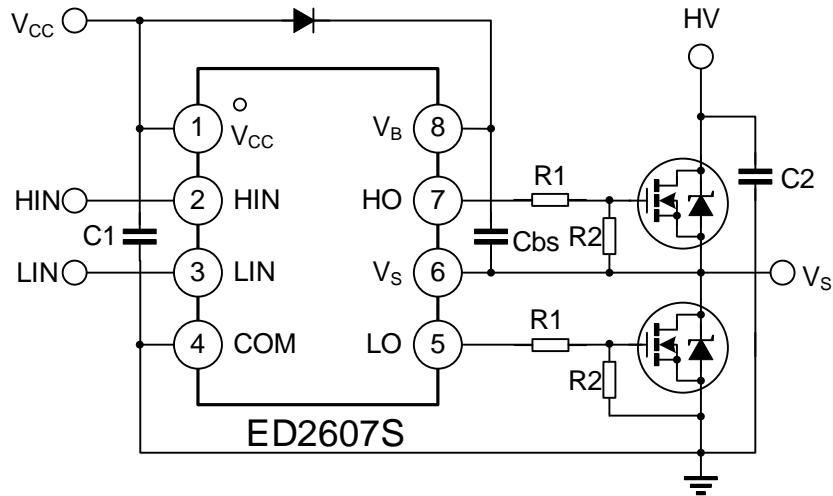


Figure 1-1 Typical Application Diagram of ED2607S

C1: Power filter capacitor; 10μF optional; as close to the chip pin as possible.

C2: High-voltage power filter capacitor. The capacitance depends on the application of circuit.

R1: Gate drive resistor. The resistance depends on the device being driven. 33~100Ω is recommended.

R2: MOS gate and source resistor. 10k~33kΩ is recommended.

D<sub>bs</sub>: Bootstrap diodes. Those with high reverse breakdown voltage (>600V) and short recovery time are preferred.

C<sub>bs</sub>: Bootstrap capacitors. Ceramic capacitors or tantalum capacitors are preferred. The minimum capacitance is calculated as follows:

$$C_{bs} \geq 15 \cdot \frac{2 \cdot [2 \cdot Q_g + Q_{period} + \frac{I_{bs(staic)}}{f} + \frac{I_{bs(leak)}}{f}]}{V_{CC} - V_F - V_{ds(L)}}$$

Where Q<sub>g</sub> is the gate charge of high-side power device;

Q<sub>period</sub> is the gate charge required by level-switching circuit in each cycle, which is about 10nC;

I<sub>bs(staic)</sub> is the static current of the high-side drive circuit;

I<sub>bs(leak)</sub> is the leakage current of the bootstrap capacitor;

F is the operating frequency of the circuit;

V<sub>CC</sub> is the low-side supply voltage;

V<sub>F</sub> is the forward turn-on voltage drop of the bootstrap diode;

V<sub>ds(L)</sub> is the turn-on voltage drop of the low-side power device.

Note: The above circuits and parameters are for reference only. The actual circuit shall be designed with the measured results.

## 1.6 Functional Block Diagram

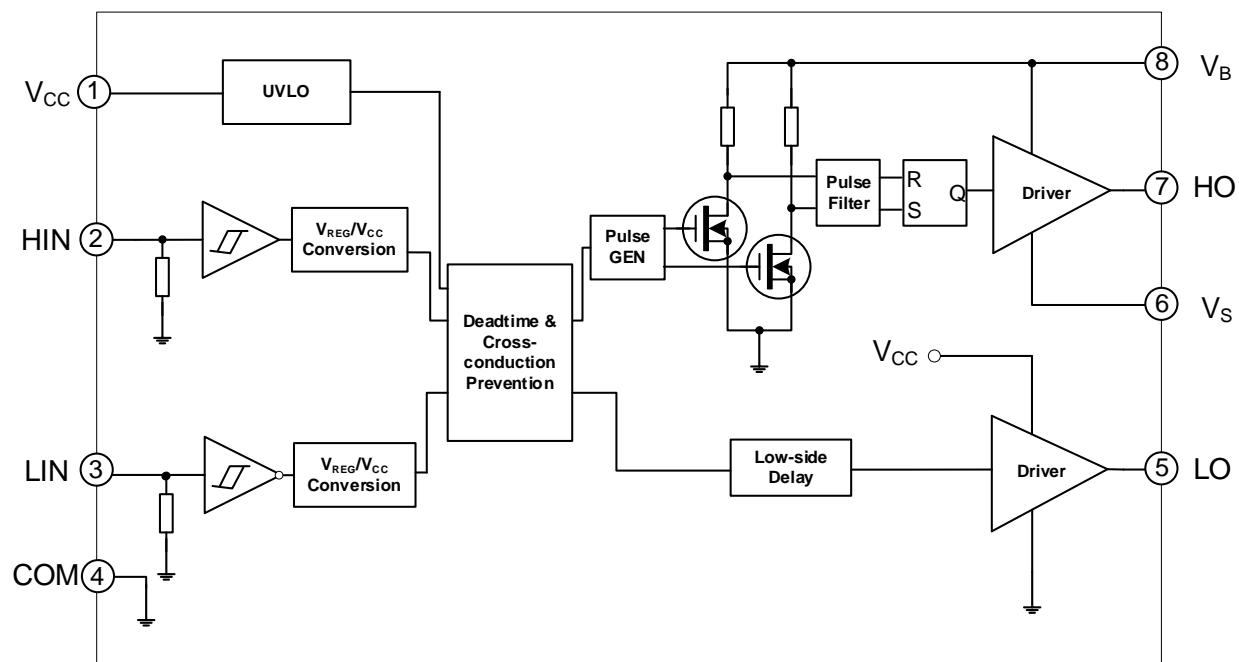


Figure 1-2 Functional Block Diagram of ED2607S

## 1.7 Pin Definitions

### 1.7.1 ED2607S Pin Diagram

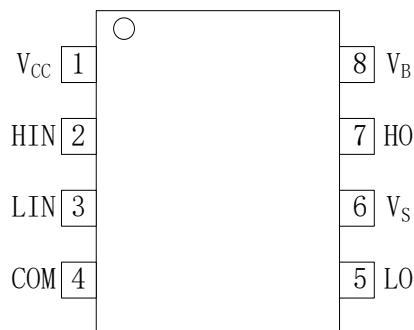


Figure 1-3 Pin Diagram of ED2607S

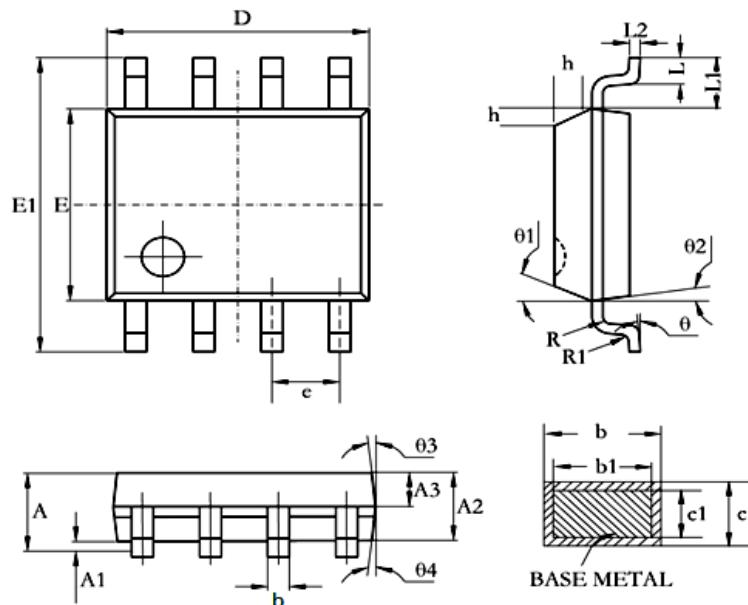
### 1.7.2 ED2607S Pin Descriptions

Table 1-1 ED2607S Pin Descriptions

Pin	Name	Description
1	V <sub>CC</sub>	Low-side Power Supply
2	HIN	High-side Input
3	LIN	Low-side Input
4	COM	Ground
5	LO	Low-side Output
6	V <sub>S</sub>	High-side Floating Offset Voltage
7	HO	High-side Output
8	V <sub>B</sub>	High-side Floating Absolute Voltage

## 2 Package Information

### 2.1 ED2607S SOP8



Symbol	Dimensions in mm			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.36	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.25	1.40	1.65	0.049	0.055	0.065
A3	0.50	0.60	0.70	0.020	0.024	0.028
b	0.38	-	0.51	0.015	-	0.020
b1	0.37	0.42	0.47	0.015	0.017	0.019
c	0.17	-	0.25	0.007	-	0.010
c1	0.17	0.20	0.23	0.007	0.008	0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	5.80	6.00	6.20	0.228	0.236	0.244
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC					
L	0.45	0.60	0.80	0.018	0.024	0.031
L1	1.04REF					
L2	0.25BSC					
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
h	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	-	8°	0°	-	8°
θ1	15°	17°	19°	15°	17°	19°
θ2	11°	13°	15°	11°	13°	15°
θ3	15°	17°	19°	15°	17°	19°
θ4	11°	13°	15°	11°	13°	15°

Product Number	Package Type	Marking ID	Package Method	Quantity
ED2607S	SOP8	ED2607S	Tape & Reel	3000

### 3 Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

(All pins are referenced to COM unless otherwise specified.)

Parameter	Symbol	Min. ~ Max.	Unit
High-side Floating Absolute Voltage	V <sub>B</sub>	-0.3~625	V
High-side Floating Offset Voltage	V <sub>S</sub>	V <sub>B</sub> -25~V <sub>B</sub> +0.3	V
High-side Output Voltage	V <sub>HO</sub>	V <sub>S</sub> -0.3~V <sub>B</sub> +0.3	V
Low-side Power Supply	V <sub>CC</sub>	-0.3~25	V
Low-side Output Voltage	V <sub>LO</sub>	-0.5~V <sub>CC</sub> +0.3	V
Logic Input Voltage (HIN, LIN)	V <sub>IN</sub>	-0.3~6.5	V
Swing Rate of Offset Voltage	dV <sub>S</sub> /dt	≤50	V/ns
Power Dissipation @T <sub>A</sub> ≤25°C	P <sub>D</sub>	≤0.625	W
Junction-to-Ambient Thermal Resistance	R <sub>thJA</sub>	≤200	°C/W
Junction Temperature	T <sub>j</sub>	≤150	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

Notes:

- In any case, power dissipation shall not exceed P<sub>D</sub>.
- The chip may get damaged if it operates under voltages above the absolute maximum ratings.

#### 3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

(All voltages are referenced to COM unless otherwise specified.)

Parameter	Symbol	Min.	Max.	Unit
High-side Floating Absolute Voltage	V <sub>B</sub>	V <sub>S</sub> +10	V <sub>S</sub> +20	V
High-side Floating Offset Voltage	V <sub>S</sub>	-5	600	V
High-side Output Voltage	V <sub>HO</sub>	V <sub>S</sub>	V <sub>B</sub>	V
Low-side Power Supply	V <sub>CC</sub>	10	20	V
Low-side Output Voltage	V <sub>LO</sub>	0	V <sub>CC</sub>	V
Logic Input Voltage (HIN, LIN)	V <sub>IN</sub>	0	5.5	V
Ambient Temperature	T <sub>A</sub>	-40	125	°C

Note: The reliability may get affected if the chip operates in an environment that exceeds the recommended conditions for a long period of time.

### 3.3 Static Electrical Characteristics

Table 3-3 Static Electrical Characteristics

[ $T_A = 25^\circ C$ ,  $V_{BIAS} (V_{CC}, V_{BS}) = 15V$  and  $V_S = COM$  unless otherwise specified.]

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
High-level Input Threshold Voltage	$V_{IH}$	$V_{CC} = 10V$ to $20V$	2.7	-	-	V
Low-level Input Threshold Voltage	$V_{IL}$		-	-	0.8	
High-level Output Voltage $V_{BIAS} - V_O$	$V_{OH}$	$I_O = 20mA$	-	0.7	1.2	
Low-level Output Voltage $V_O$	$V_{OL}$		-	0.2	0.35	
Leakage Current of Floating Power Supply	$I_{LK}$	$V_B = V_S = 600V$	-	1	5	uA
$V_{BS}$ Quiescent Current	$I_{QBS}$	$V_{IN} = 0V$ or $5V$	-	50	90	
$V_{CC}$ Quiescent Current	$I_{QCC}$		-	210	380	
High-level Input Bias Current	$I_{IN+}$	$V_{IN} = 5V$	-	25	50	
Low-level Input Bias Current	$I_{IN-}$	$V_{IN} = 0V$	-	-	1	
$V_{CC}$ Threshold Voltage	$V_{CCUV+}$		8.3	9.2	10.1	V
$V_{CC}$ Turn-off Voltage	$V_{CCUV-}$		7.6	8.4	9.2	
$V_{CC}$ Hysteresis Voltage	$V_{CCUVH}$		0.4	0.8	-	
High-level Output Short-circuit Pulse Current	$I_{O+}$	$V_O = 0V$ ; $PW \leq 10\mu s$	140	250	-	mA
Low-level Output Short-circuit Pulse Current	$I_{O-}$	$V_O = 15V$ ; $PW \leq 10\mu s$	250	410	-	

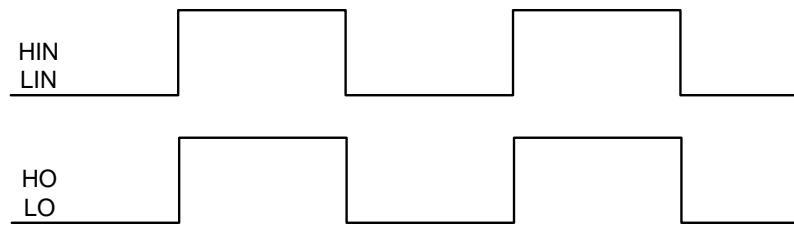
### 3.4 Dynamic Electrical Characteristics

Table 3-4 Dynamic Electrical Characteristics

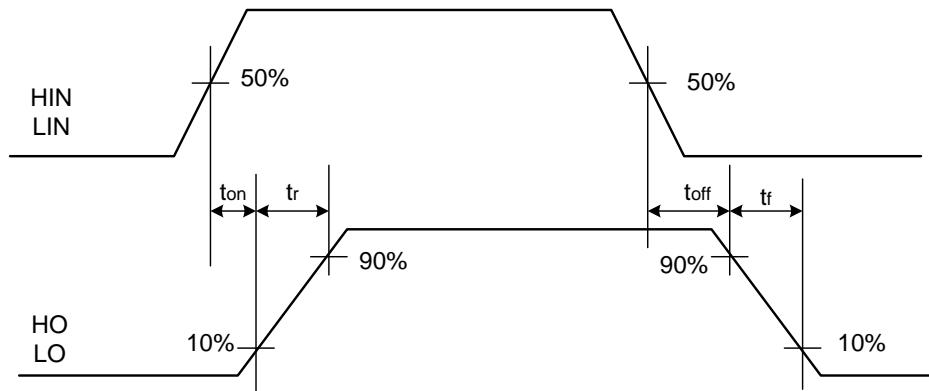
[ $T_A = 25^\circ C$ ,  $V_{BIAS} (V_{CC}, V_{BS}) = 15V$ ,  $C_L = 1000pF$  and  $V_S = COM$  unless otherwise specified.]

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on Propagation Delay	$t_{on}$	$V_S = 0V$	--	90	160	ns
Turn-off Propagation Delay	$t_{off}$		--	110	180	
High-low Side Delay Match	MT		--	0	50	
Turn-on Rise Time	$t_r$		--	85	130	
Turn-off Fall Time	$t_f$		--	45	80	
Deadtime	DT		--	360	510	

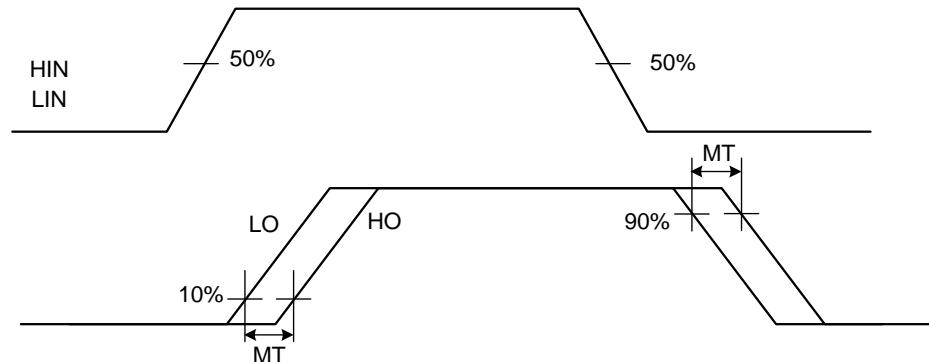
#### 4 Logic Function Timing Diagram



#### 5 Propagation Delay Test Standards

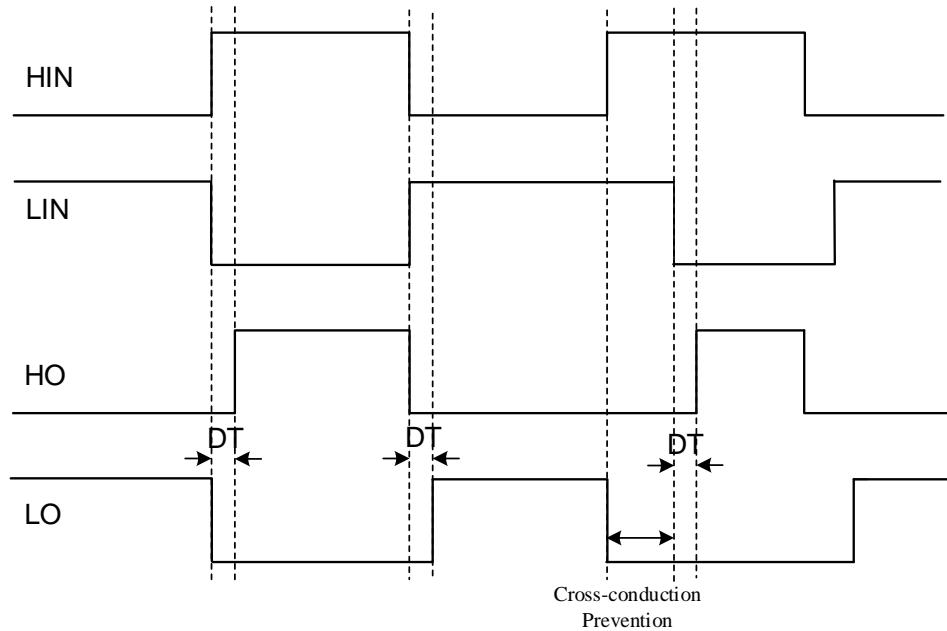


#### 6 Propagation Delay Matching Test Standards



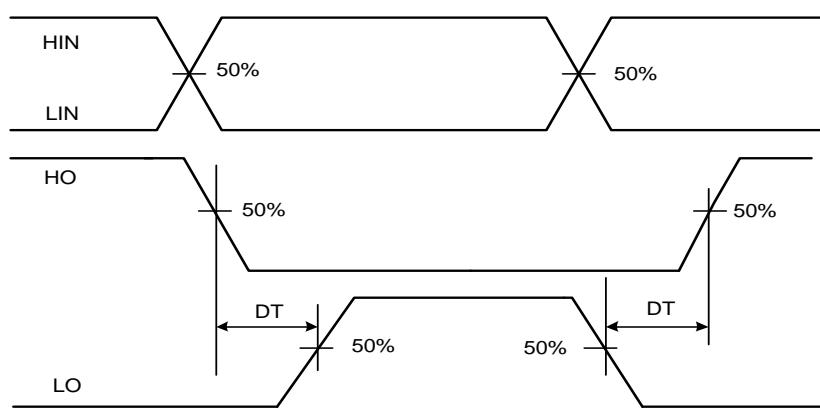
## 7 Cross-conduction Prevention

A protection circuit is specially designed inside the chip to enable cross-conduction prevention feature, which effectively prevents MOSFETs or IGBTs from damage when high-side and low-side input signals are interfered. The figure below shows how the protection circuit works.



## 8 Deadtime

The chip is designed with dedicated deadtime protection circuit. During deadtime, both the high-side and low-side outputs are set to LOW. This feature prevents both MOSFETs or IGBTs of each half-bridge from switching on at the same time. The following figure shows the timing relationship between deadtime, input signal and output signal.



## 9 Revision History

Rev.	Description	Date	Prepared By
V0.1	First release.	2021/07/09	Michelle Xie
V0.2	<ol style="list-style-type: none"><li>Updated Logic Function Timing Diagram;</li><li>Added Cross-conduction Prevention and Deadtime;</li><li>Added R2 resistor and detailed descriptions in Typical Application Diagram;</li><li>Proofread some descriptions in Overview and Features;</li><li>Corrected some parameter names in section 3 Electrical Characteristics;</li></ol>	2023/05/22	Lay Ye/ Eric Deng
V1.0	<ol style="list-style-type: none"><li>Corrected some grammar mistakes and wrong sentences;</li><li>Standardized document format.</li></ol>	2023/05/26	Eric Deng

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