

# **Datasheet**

## **FD2004D**

### **24V Half-bridge Gate Driver**

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**Table of Content**

1 System Introduction.....	3
1.1 Overview .....	3
1.2 Applications.....	3
1.3 Characteristics .....	3
1.4 Packaging .....	3
1.5 Pinout of the chip.....	4
1.5.1 Pin Description.....	4
1.6 Circuit block diagram.....	4
1.7 Typical application circuit .....	5
1.8 Logic Timing Diagram .....	5
1.9 Test criteria for switching time .....	6
1.10 Test criteria for transmission time matching.....	6
1.11 Test criteria for the time shutdown enabling.....	6
2 Package size.....	7
2.1 DFN8(3*3) .....	7
3 Ordering Information.....	8
4 Electrical Characteristics .....	9
4.1 Absolute Maximum Ratings .....	9
4.2 Recommended Operating Conditions.....	10
4.3 Electric parameters .....	10
5 Copyright Notice.....	12

## FD2004D 24V Half-bridge Gate Driver

### 1 System Introduction

#### 1.1 Overview

The FD2004D is a half-bridge gate drive IC designed for driving N-type MOSFETs at high frequency and speed with integrated bootstrap diodes. The FD2004D has a built-in under voltage (UVLO) protection function which prevents the MOSFET from operating at too low voltage and improves efficiency. The FD2004D has built-in pass-through prevention and dead time settings to prevent the MOSFETs on the high and low side of the drive from passing straight through, which can effectively protecting the power device. The FD2004D integrates the enable & shutdown functions for simultaneous shutdown of hi-channel and lo-channel outputs.

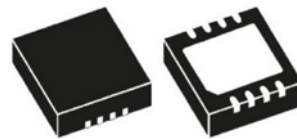
#### 1.2 Applications

- Half/full bridge converters
- Double-ended Forward Converters
- Motor drive

#### 1.3 Characteristics

- Absolute voltage of suspension: +20V
- Built-in bootstrap diode
- Supply voltage: 4.4 ~ 16V
- Compatible voltages for input logic: 3.3V/5V
- VCC undervoltage protection (UVLO)
- Built-in dead time
- Integrated enable shutdown function
- High side output in phase with the input, low side output out of phase with the input
- High and low channel matching

#### 1.4 Packaging



DFN8(3\*3)

## 1.5 Pinout of the chip

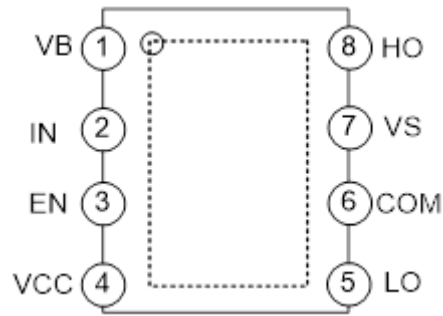


Figure 1-1 Pinout of the FD2004D

### 1.5.1 Pin Description

Pin number	Pin Name	Pin Description
1	VB	Floating absolute voltage on the high side
2	IN	Input
3	EN	Enabled switch-off input
4	VCC	Supply voltage on low side
5	LO	Output on the low side
6	COM	Grounding
7	VS	Floating offset voltage on the high side
8	HO	Output on the high side

Table 1-1 FD2004D DFN8(3\*3) 1.5.1 Pin Description

### 1.6 Circuit block diagram

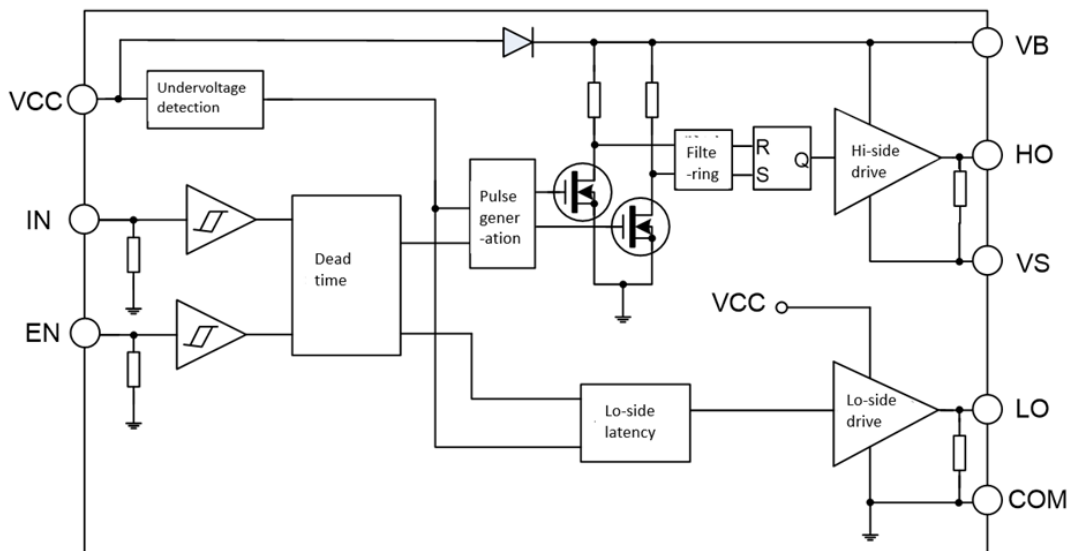


Figure1-2 Circuit Block Diagram of FD2004D

### 1.7 Typical application circuit

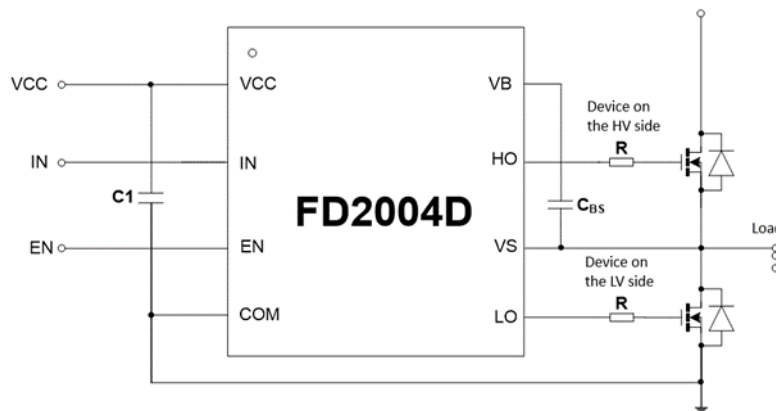


Figure 1-3 FD2004D Typical application circuit

Notes:

- [1] C1: Power supply filter capacitor, depending on the circuit, can be selected from  $1\mu\text{F} \sim 10\mu\text{F}$ ;
- [2] R: Gate drive resistor, resistance value depends on the driven device;
- [3] C<sub>BS</sub>: Bootstrap capacitor. Ceramic or tantalum capacitors should be selected from  $0.1\mu\text{F} \sim 10\mu\text{F}$ .

### 1.8 Logic Timing Diagram

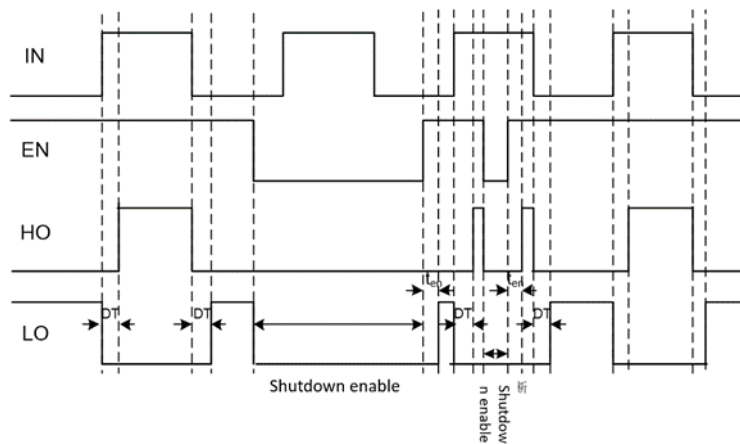


Figure 1-4 FD2004D Logic Timing Diagram

**1.9 Test criteria for switching time**

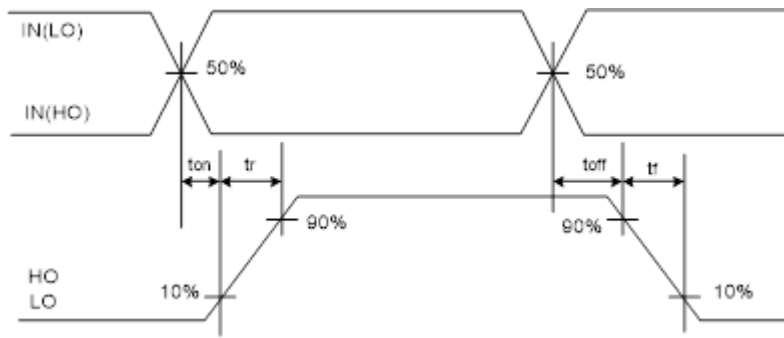


Figure 1-5 FD2004D Test criteria for switching time Diagram

**1.10 Test criteria for transmission time matching**

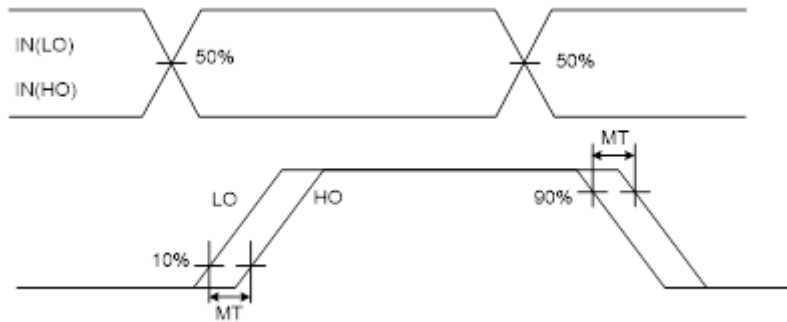


Figure 1-6 FD2004D Test criteria for transmission time matching Diagram

**1.11 Test criteria for the time shutdown enabling**

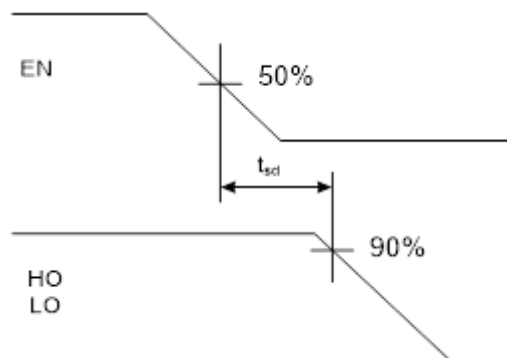


Figure 1-7 FD2004D Test criteria for the time shutdown enabling Diagram

## 2 Package size

### 2.1 DFN8(3\*3)

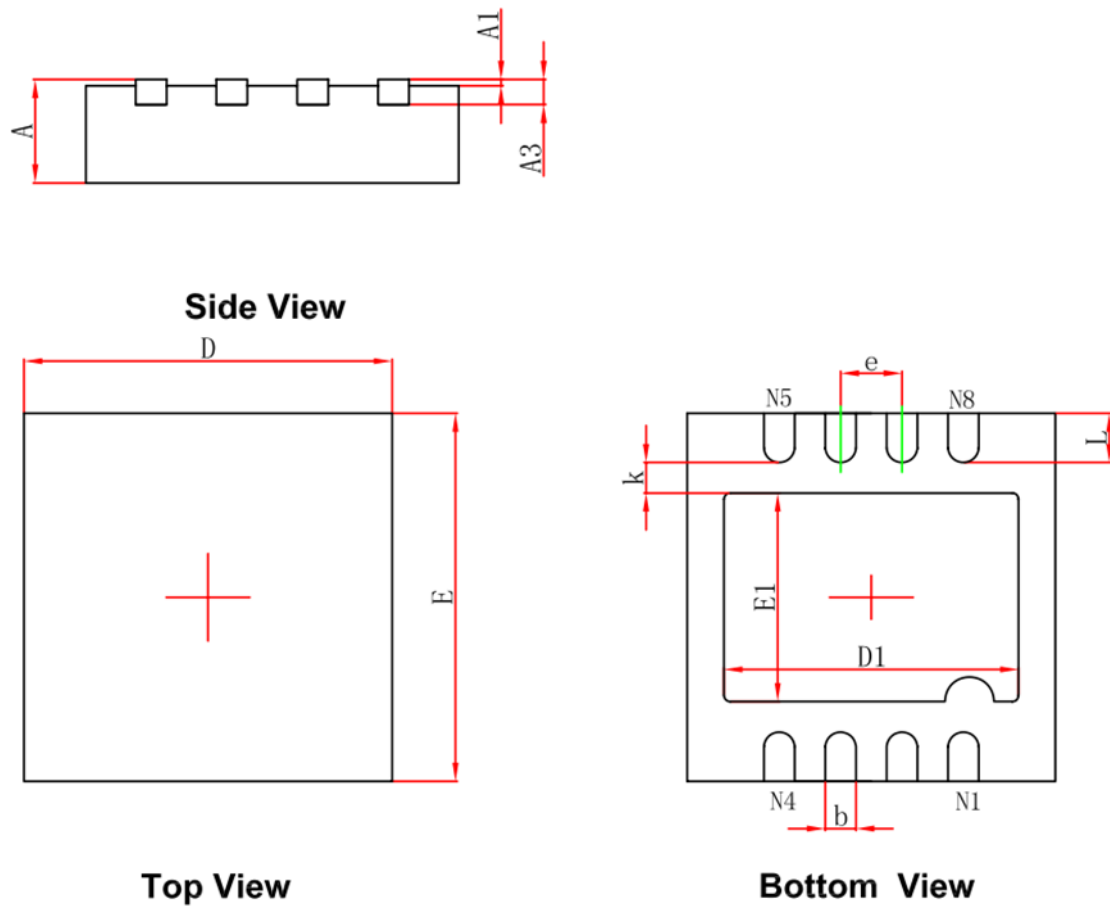


Figure 2-1 DFN8(3\*3) Package Outline Dimensions

Table 2-1 Package Size Table of DFN8(3\*3)

Symbol	Dimensions In Millimeter			
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1		0.050		0.002
A3	0.203REF		0.008REF	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.300	2.500	0.091	0.098
E1	1.600	1.800	0.063	0.071
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.800	0.012
e	0.500TYP		0.020TYP	
l	0.324	0.476	0.013	0.019

### 3 Ordering Information

Table 3-1 Model Options

<b>Model number</b>	<b>Form of package</b>	<b>Marking</b>	<b>Packaging</b>	<b>Quantity</b>
FD2004D	DFN8(3*3) (Example)	FD2004D (Example)	Tape & Reel (Example)	5000 (Example)



## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings

 Table 4-1 Absolute Maximum Ratings<sup>[1]</sup>

(Unless otherwise stated, all pins are referenced to COM)

Parameters	Symbols	Range	Unit
Floating absolute voltage on the high side	$V_B$	-0.3 ~ 24	V
High-side floating offset voltage	$V_S$	$V_B - 16 \sim V_B + 0.3$	V
High-side output voltage	$V_{HO}$	$V_S - 0.3 \sim V_B + 0.3$	V
Low side supply voltage	$V_{CC}$	-0.3 ~ 16	V
Low-side output voltage	$V_{LO}$	-0.3 ~ $V_{CC} + 0.3$	V
Logic input voltage (IN, EN)	$V_{IN}$	-0.3 ~ 6.5	V
Range of offset voltage swings	$dV_S/dt$	$\leq 50$	V/ns
Power consumption @ $T_A \leq 25^\circ\text{C}$	DFN8 PD	2.5	W
Thermal resistance of the junction to environment	DFN8 $R_{thJA}$	50	$^\circ\text{C}/\text{W}$
Junction temperature range	$T_j$	$\leq 150$	$^\circ\text{C}$
Environmental temperature of operation	$T_A$	-40 ~ 125	$^\circ\text{C}$
Temperature range for storage	$T_{stg}$	-55 ~ 150	$^\circ\text{C}$

Notes:

- [4] Voltage exceeding the absolute maximum rating may damage the chip;
- [5] In any case, do not exceed the PD.

## 4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

(All voltages are referred to COM)

Parameters	Symbols	Minimum	Maximum	Unit
High-side floating absolute voltage	$V_{BS}$	$V_S + 4.4$	$V_S + 16$	V
Floating offset voltage on static high side	$V_{SN}$	-3	20	V
High-side output voltage	$V_{HO}$	$V_S$	$V_B$	V
Low-side supply voltage	$V_{CC}$	4.4	16	V
Low-side output voltage	$V_{LO}$	0	$V_{CC}$	V
Logic input voltage (IN, EN)	$V_{IN}$	0	6.0	V
Environmental temperature	$T_A$	-40	125	°C

## 4.3 Electric parameters

Table 4-3 Global Electrical Characteristics

 ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 15\text{V}$ , unless otherwise specified)

Parameters	Symbol	Test Condition	Minimum	Typical	Maximum	Unit
<b>Power supply current</b>						
VCC operating voltage range	$V_{CC}$		4.4	--	16	V
VCC static current	$I_{QCC}$	$V_{EN} = 0\text{V}$	--	0.56	0.8	mA
Leakage currents in suspended power	$I_{LK}$	$V_B = V_S = 20\text{V}$	--	0.1	5.0	$\mu\text{A}$
<b>Input IN/EN</b>						
Hi-level input threshold voltage	$V_{IH}$		2.7	2.2	--	V
Lo-level input threshold voltage	$V_{IL}$		--	1.4	0.8	V
Hi-level input bias current	$I_{IN/EN+}$	$V_{IN/EN} = 5\text{V}$	--	65	100	$\mu\text{A}$
Lo-level input bias current	$I_{IN/EN-}$	$V_{IN/EN} = 0\text{V}$	--	--	2	$\mu\text{A}$
<b>UVLO</b>						
VCC opening voltage for undervoltage protection	$V_{CCUV+}$		3.4	3.9	4.4	V
VCC switch-off voltage for undervoltage protection	$V_{CCUV-}$		3.2	3.7	4.2	V
VCC hysteresis voltage for undervoltage protection	$V_{CCUVH}$		--	0.2	--	V
<b>Bootstrap diode</b>						
Forward voltage	$V_{F1}$	$I_S = 10\text{mA}$	---	0.75	---	V
	$V_{F2}$	$I_S = 50\text{mA}$	---	0.95	---	V
<b>High-end output</b>						
High-level output voltage	$V_{OHH}$	$I_O = -100\text{mA}$	--	0.2	0.36	V

Parameters	Symbol	Test Condition	Minimum	Typical	Maximum	Unit
Low-level output voltage	$V_{OLH}$	$I_O = 100\text{mA}$	--	0.1	0.18	V
High-level output short-circuit pulse current	$I_{OHH}$	$V_O = 0\text{V}$	2.0	3.2	--	A
Low-level output short-circuit pulse current	$I_{OLH}$	$V_O = 12\text{V}$	2.0	3.0	--	A
<b>Low-end output</b>						
High-level output voltage	$V_{OHL}$	$I_O = -100\text{mA}$	--	0.2	0.36	V
Low-level output voltage	$V_{OLL}$	$I_O = 100\text{mA}$	--	0.1	0.18	V
High-level output short-circuit pulse current	$I_{OHL}$	$V_O = 0\text{V}$	2.0	3.2	--	A
Low-level output short-circuit pulse current	$I_{OLL}$	$V_O = 12\text{V}$	2.0	3.0	--	A
<b>Switching time parameters</b>						
Transmission time of the output rising edge	$t_{on}$		--	80	--	ns
Transmission time of the output falling edge	$t_{off}$		--	40	--	ns
Deadtime	DT		--	50	--	ns
Transmission time of the output rising edge	$t_r$	$C_L = 3000\text{pF}$	--	45	--	ns
Transmission time of the output falling edge	$t_f$	$C_L = 3000\text{pF}$	--	40	--	ns
High and low-side delay matching	MT		--	--	30	ns
Delay time for enabling shutdown	$t_{sd}$		--	40	--	ns

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