Datasheet

Three-phase Bridge Driver

FD6288T&Q

Fortior Technology (Shenzhen) Co., Ltd.

Content

FD6288T&Q Three-phase Bridge Driver

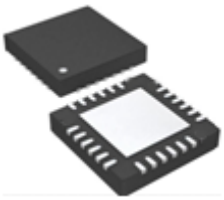
1 System Introduction

1.1 Overview

FD6288T&Q is an integrated three-span half-bridge gate driver IC designed for high voltage and high speed drive MOSFETs that operate up to +250V. The special HVIC technology realizes stable monolithic structure. Logic inputs are compatible with CMOS or LSTTL outputs, and the logic voltage can be down to 3.3V. The output driver has a high pulse current buffer stage, which achieves a minimum driver impedance. Propagation delays are matched to simplify use in high frequency applications. Floating channel can be used to drive N-channel power MOSFET with high-end configuration, working voltage up to 250V.

1.2 Packages

TSSOP-20



QFN-24

1.3 Features

- Fully operational to +250V
- Gate driver supply range from 5V to 20V
- Independent Three half-bridge drivers
- 3.3V and 5V logic input compatible
- Undervoltage lockout for all channels
- Cross-conduction prevention logic
- Internal set dead-time
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant

1.4 Applications

- Motor drives
- DC-AC inverter drives

1.5 Functional Block Diagram

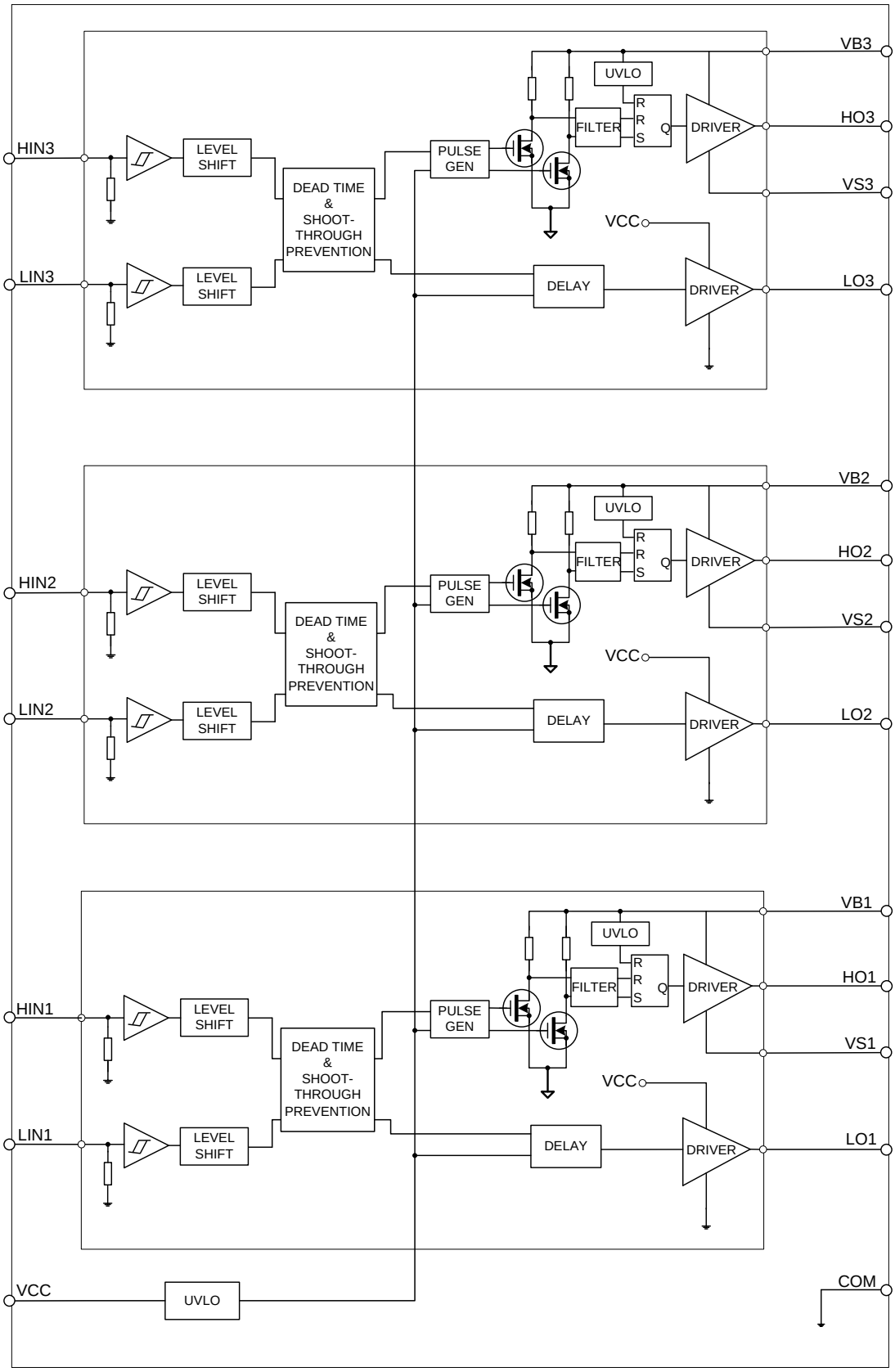


Figure 1-1 Functional Block Diagram of FD6288T&Q

1.6 Pin Diagrams

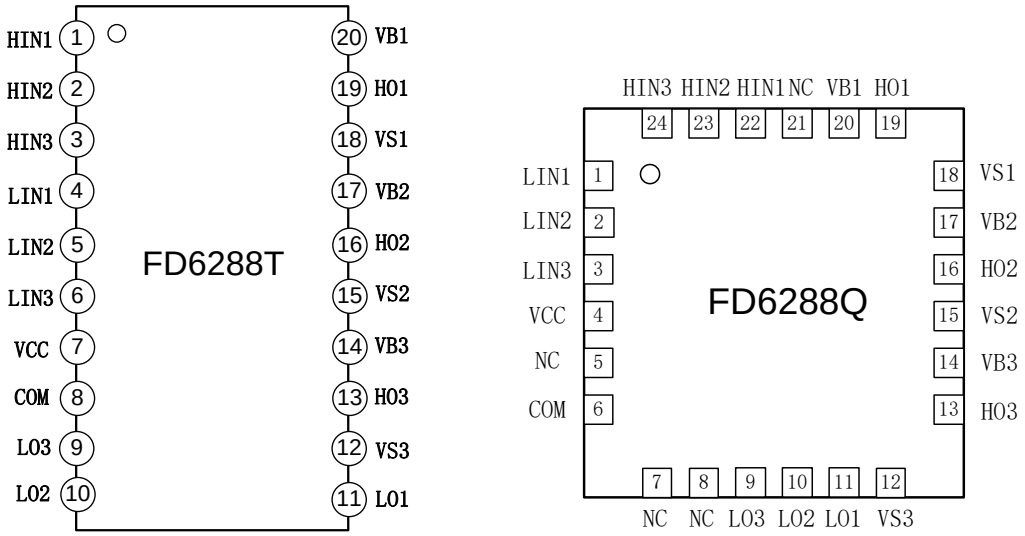


Figure 1-2 Pin Diagram of FD6288T&Q

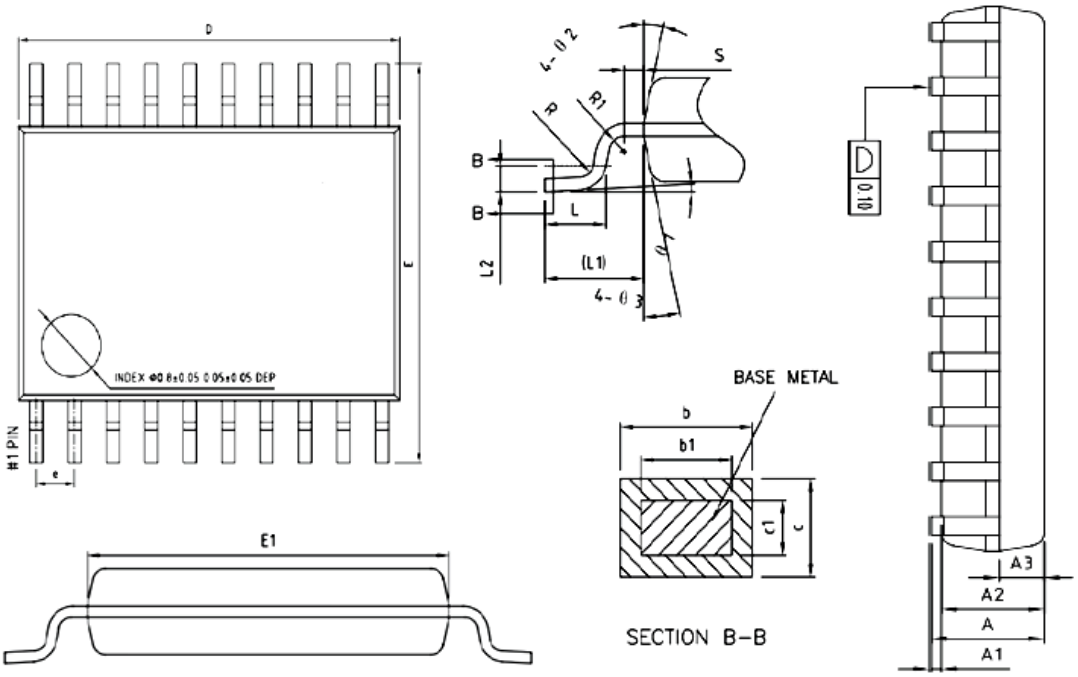
1.7 Pin Definitions

Table 1-1 FD6288T&Q Pin Descriptions

Symbol	Description
V_{CC}	Low-side and logic fixed supply
HIN1,2,3	Logic input for high side gate driver output(HO),in phase
LIN1,2,3	Logic input for low side gate driver output(LO),in phase
COM	Low-side return
LO1,2,3	Low-side gate drive output
$V_{S1,2,3}$	High-side floating supply return
HO1,2,3	High-side gate drive output
$V_{B1,2,3}$	High-side floating supply

2 Package Information

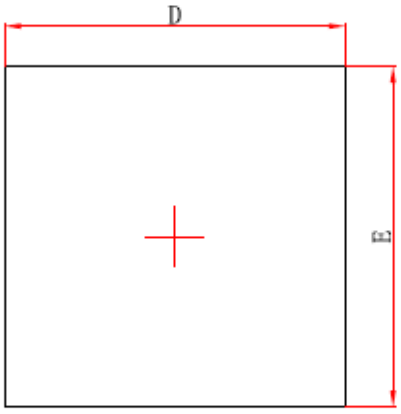
2.1 FD6288T TSSOP20



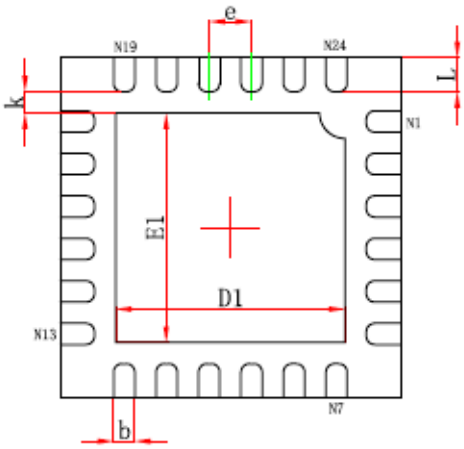
Symbol	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		

Product Number	Package Type	Marking ID	Package Method	Quantity
FD6288T	TSSOP20	FD6288T	Tape & Reel	3000

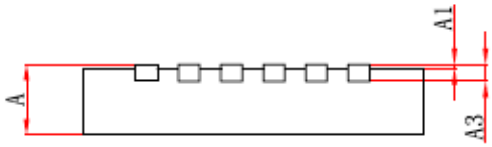
2.2 FD6288Q QFN24



Top View



Bottom View



Side View

Symbol	Dimensions in mm		Dimensions in inch	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.0031/0.0035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
K	0.200MN		0.008MN	
B	0.200	0.300	0.008	0.012
E	0.500TYP		0.020TYP	
L	0.324	0.476	0.013	0.019

Product Number	Package Type	Marking ID	Package Method	Quantity
FD6288Q	QFN24	FD6288Q	Tape & Reel	3000

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol		Min.~Max.	Units
High-side Floating Supply Voltage	$V_{B1,2,3}$		-0.3～275	V
High-side Floating Supply Offset Voltage	$V_{S1,2,3}$		$V_{B1,2,3}$-25～$V_{B1,2,3}$+0.3	V
High-side Floating Output Voltage	$V_{HO1,2,3}$		$V_{S1,2,3}$-0.3～$V_{B1,2,3}$+0.3	V
Low-side and Logic Fixed Supply Voltage	V_{CC}		-0.3～25	V
Low-side Output Voltage	$V_{LO1,2,3}$		-0.5～V_{CC}+0.3	V
Logic Input Voltage（HIN,LIN）	V_{IN}		-0.5～V_{CC}+0.3	V
Allowable Offset Supply Voltage Transient	dV_S/dt		≤50	V/ns
Package Power Dissipation @T_A≤25°C	P_D	TSSOP20	≤1.25	W
		QFN24	≤3.0	
Thermal Resistance, Junction to Ambient	R_{thJA}	TSSOP20	≤100	°C/W
		QFN24	≤42	
Junction Temperature	T_j		≤150	°C
Storage Temperature	T_{stg}		-55～150	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air condition.

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
High-side Floating Supply Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+5	$V_{S1,2,3}$+20	V
High-side Floating Supply Offset Voltage	$V_{S1,2,3}$	-4	250	V
High-side Floating Output Voltage	$V_{HO1,2,3}$	V_S	$V_{B1,2,3}$	V
Low-side and Logic Fixed Supply Voltage	V_{CC}	5	20	V
Low-side Output Voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic Input Voltage（HIN,LIN）	V_{IN}	0	V_{CC}	V
Ambient Temperature	T_A	-40	125	°C

Note: For proper operation, the device should be used within the recommended conditions. The VS offset rating is tested with all supplies biased at a 15V differential.

3.3 Static Electrical Characteristics

Table 3-3 Static Electrical Characteristics

[VBIAS (VCC, VBS1,2,3) =15V and TA =25°C unless otherwise specified.

All the parameters are referenced to COM.]

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Logic "1" Input Voltage	V_{IH}		2.7	-	-	V
Logic "0" Input Voltage	V_{IL}		-	-	0.8	
High-level Output Voltage, V_{BIAS} - V_O	V_{OH}	I_O=100mA	-	0.6	0.9	
Low-level Output Voltage, V_O	V_{OL}		-	0.3	0.45	
Offset Supply Leakage Current	I_{LK}	$V_{B1,2,3}$=$V_{S1,2,3}$=250V	-	0.1	5.0	uA
Quiescent V_{BS} Supply Current	I_{QBS}	V_{IN} =0V or 5V	-	180	270	
Quiescent V_{CC} supply Current	I_{QCC}		-	330	500	
Logic "1" Input Bias Current	I_{IN+}	V_{IN}=5V	-	25	40	
Logic "0" Input Bias Current	I_{IN-}	V_{IN}=0V	-	-	1	
V_{CC} and V_{BS} Supply Undervoltage Positive Going threshold	V_{CCUV+} V_{BSUV+}		4.2	4.6	5.0	V
V_{CC} and V_{BS} Supply Undervoltage Negative Going threshold	V_{CCUV-} V_{BSUV-}		3.9	4.3	4.7	
Output High Short Circuit Pulsed Current	I_{O+}	V_O=0V,PW≤10us	1.1	1.5	1.9	A
Output Low Short Circuit Pulsed Current	I_{O-}	V_O=15V,PW≤10us	1.3	1.8	2.3	

3.4 Dynamic Electrical Characteristics

Table 3-4 Dynamic Electrical Characteristics

[V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) =15V, C_L=1000pF and TA =25°C unless otherwise specified.]

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Turn-on Propagation Delay	ton	$V_{S1,2,3}$=0V	-	300	450	ns
Turn-off Propagation Delay	toff	$V_{S1,2,3}$=250V	-	100	160	
Delay Matching, HS & LS turn on/off	MT		-	-	30	
Turn-on Rise Time	tr		-	12	25	
Turn-off Fall Time	tf		-	12	25	
Deadtime, LS Turn-off to HS Turn-on & HS Turn-off to LS Turn-on	DT		100	200	300	

4 Typical Application Diagram

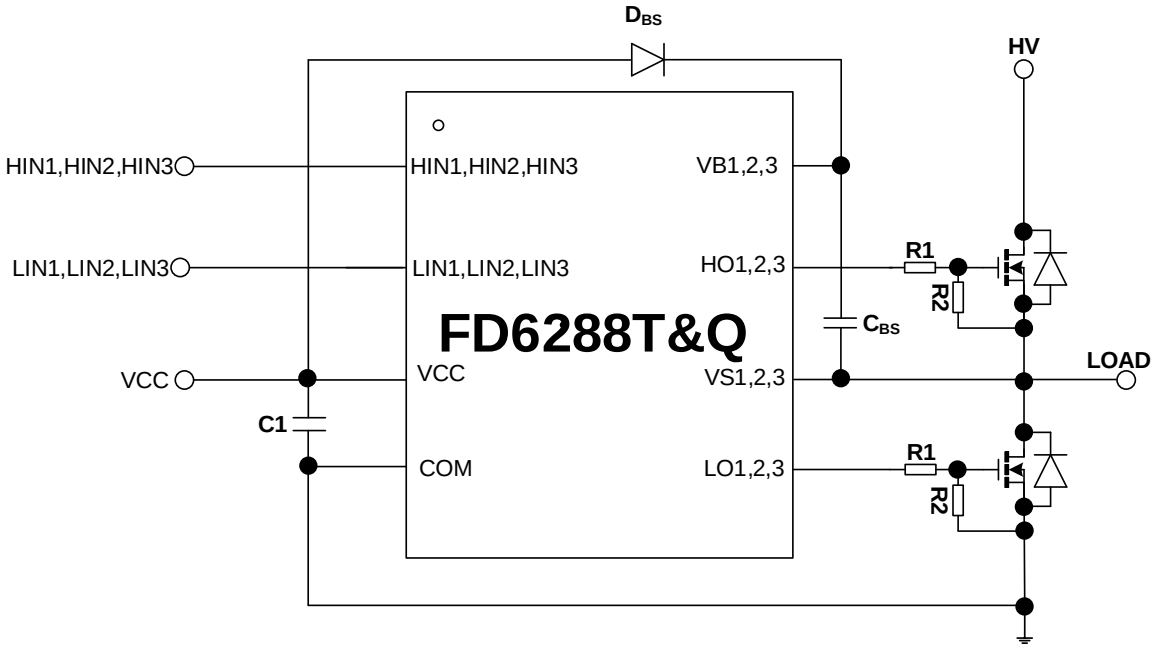


Figure 4-1 Typical Application Diagram of FD6288T&Q

C1: Power filter capacitor, according to the circuit can choose 1μF ~ 10μF, as close to the chip pin as possible.

R1: Gate drive resistor, and the resistance depends on the device being driven.

R2: MOS gate and source resistance.

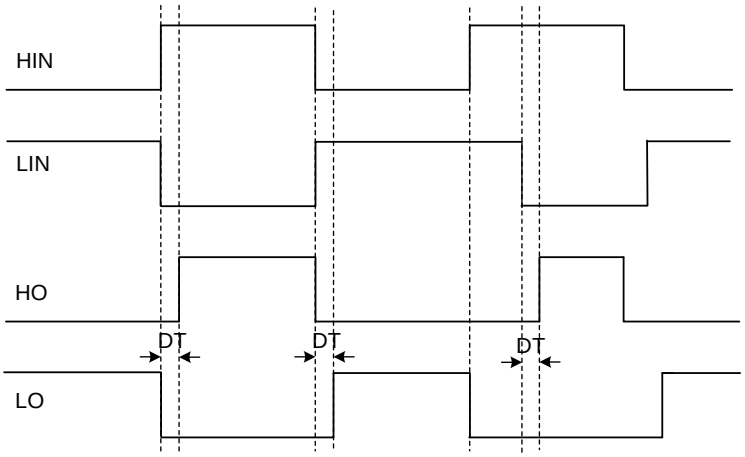
D_{BS}: Bootstrap diodes. It should be selected for high reverse breakdown voltage Schottky diodes.

C_{BS}: Bootstrap capacitors. Ceramic capacitors or tantalum capacitors should be selected, according to the circuit can choose0. 22 μ F ~ 10 μ F. The capacitor should be as close as possible to the chip pin.

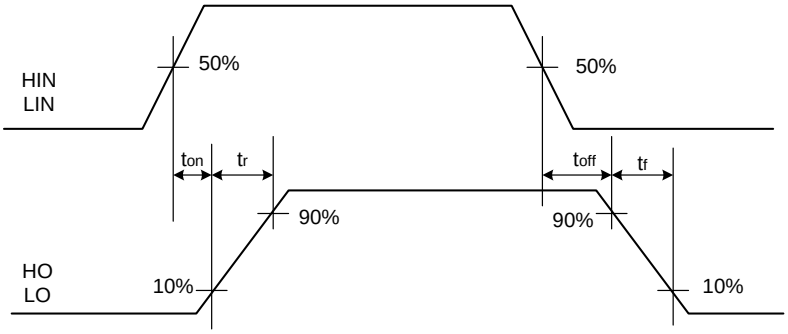
Note:

The above circuits and parameters are for reference only. The actual application circuit should be designed with the measured results in setting the parameters.

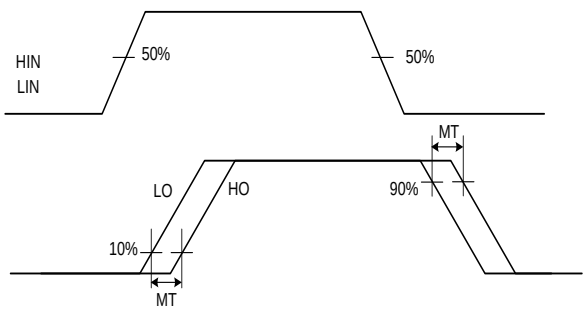
5 Input/Output Timing Diagram

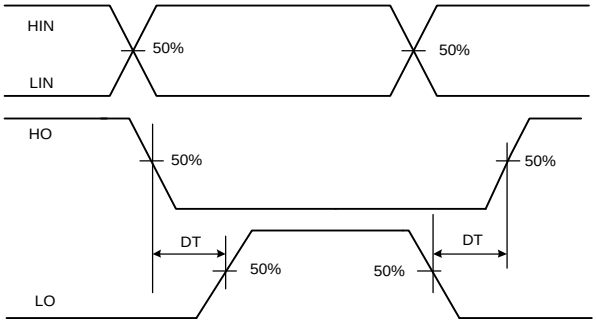


6 Switching Time Waveform Definitions



7 Delay Matching Waveform Definitions and Deadtime Waveform Definitions





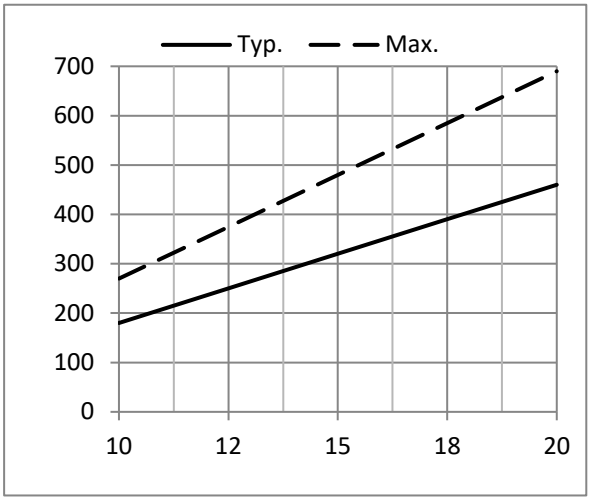


Figure 1A VCC Supply Current vs Supply Voltage

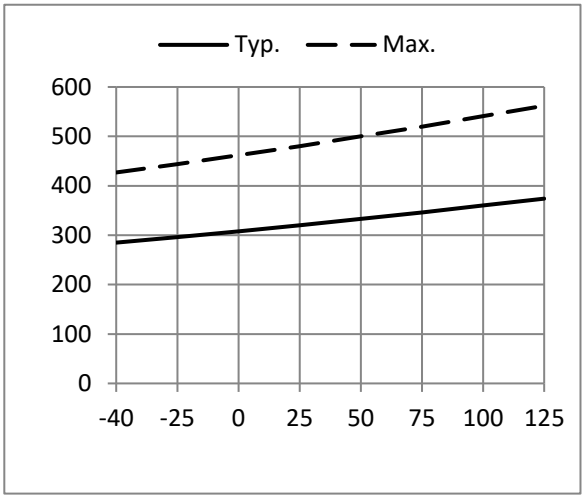


Figure 1B VCC Supply Current vs Temperature

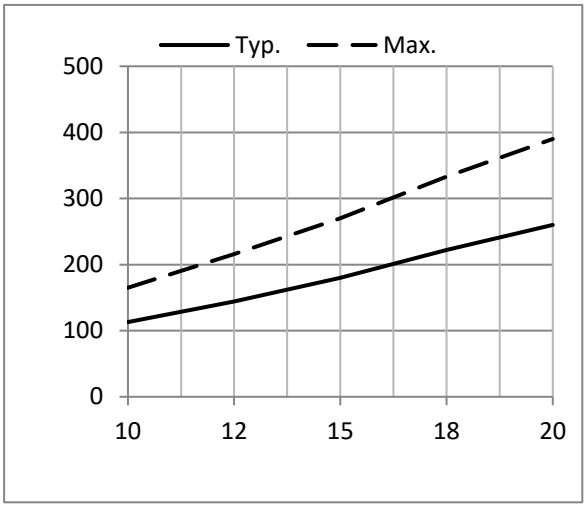


Figure 2A V_{BS} Supply Current vs Supply Voltage

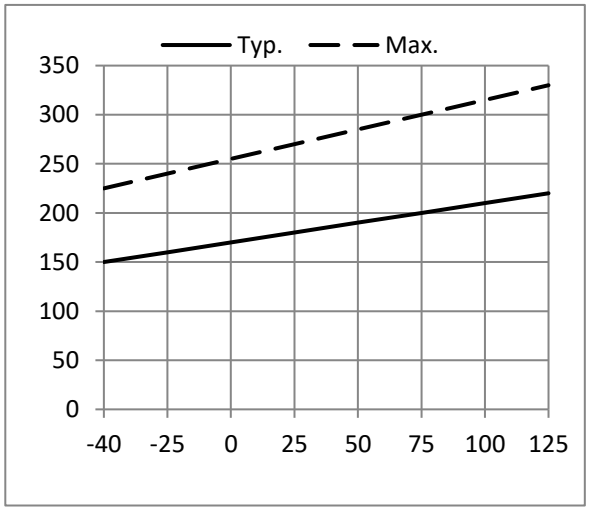


Figure 2B V_{BS} Supply Current vs Temperature

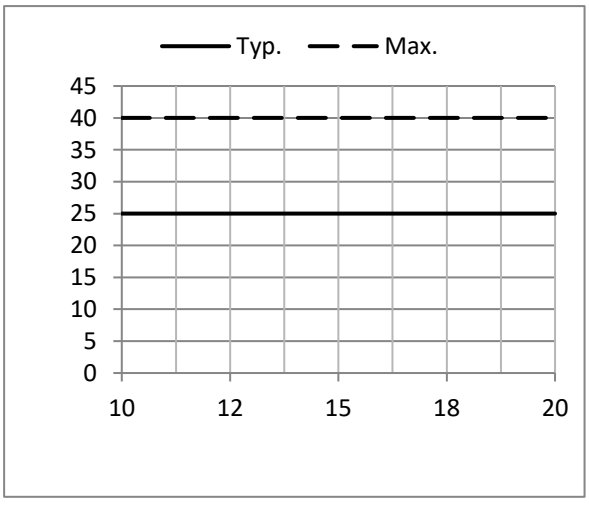


Figure 3A Logic “1” Input Current vs Supply Voltage

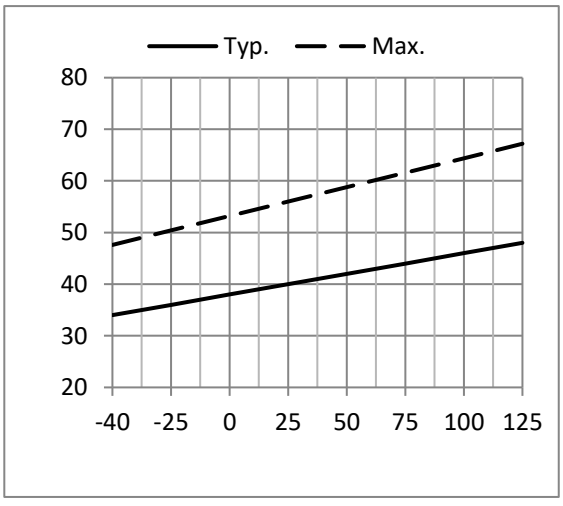


Figure 3B Logic “1” Input Current vs Temperature

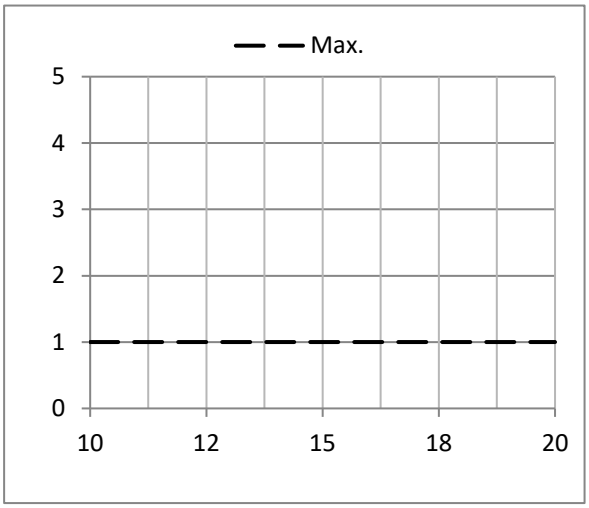


Figure 4A Logic “0” Input Current vs Supply Voltage

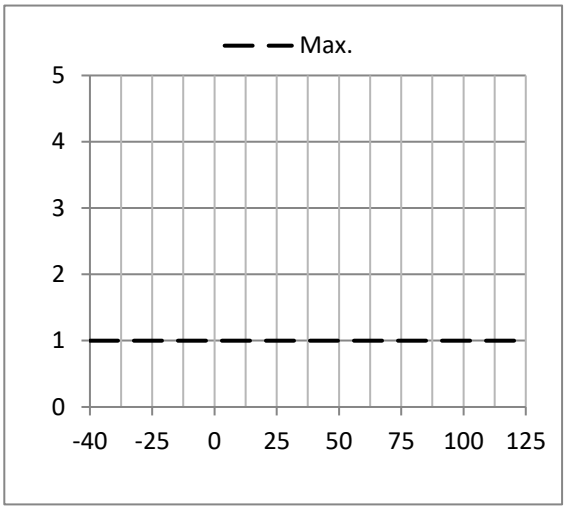


Figure 4B Logic “0” Input Current vs Temperature

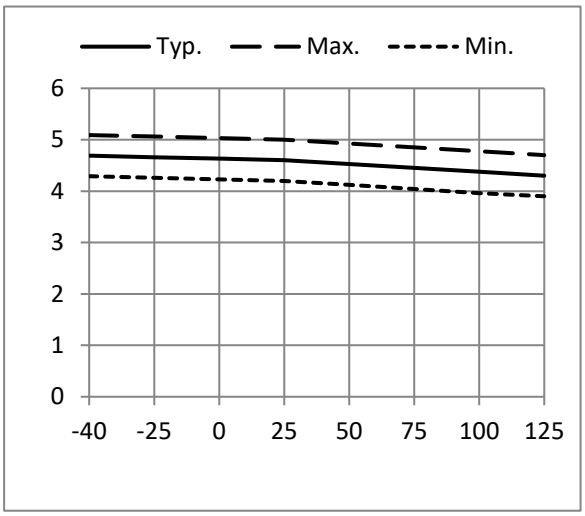


Figure 5A V_{CC} Undervoltage Threshold (+) vs Temperature

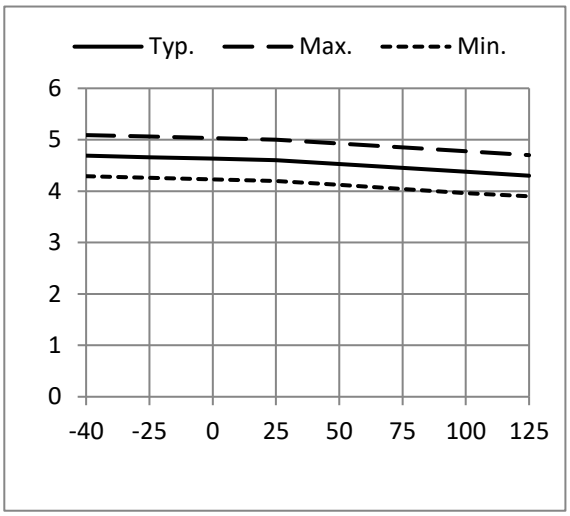


Figure 5B V_{CC} Undervoltage Threshold (-) vs Temperature

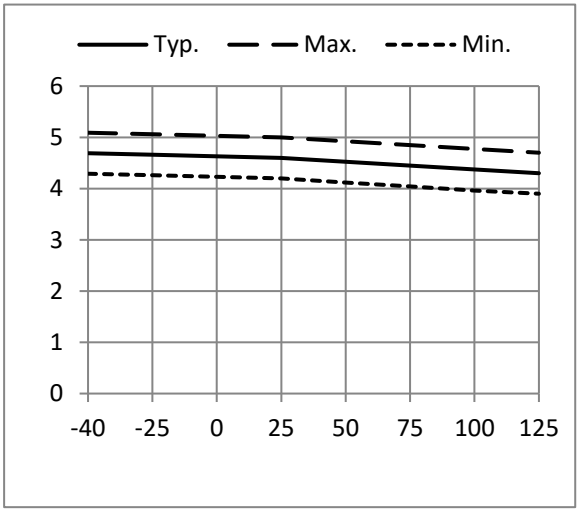


Figure 6A V_{BS} Undervoltage Threshold (+)

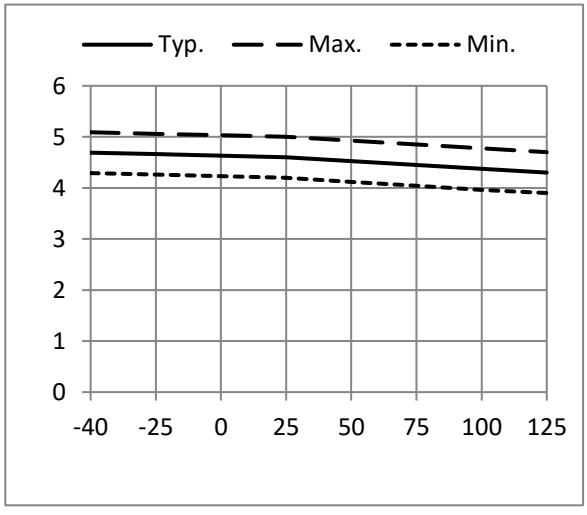


Figure 6B V_{BS} Undervoltage Threshold (-)

vs Temperature

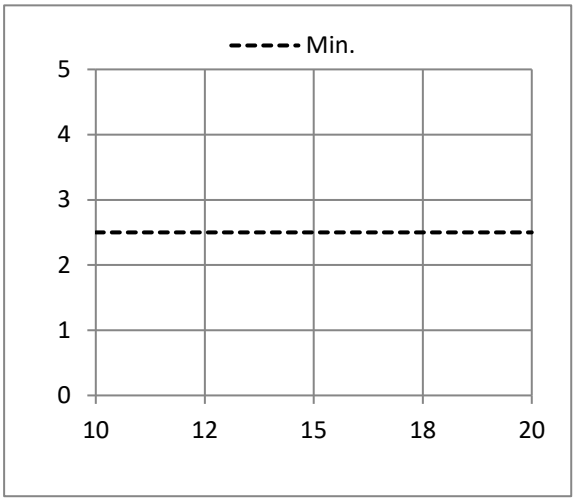


Figure 7A Logic “1” Input Voltage vs Supply Voltage

vs Temperature

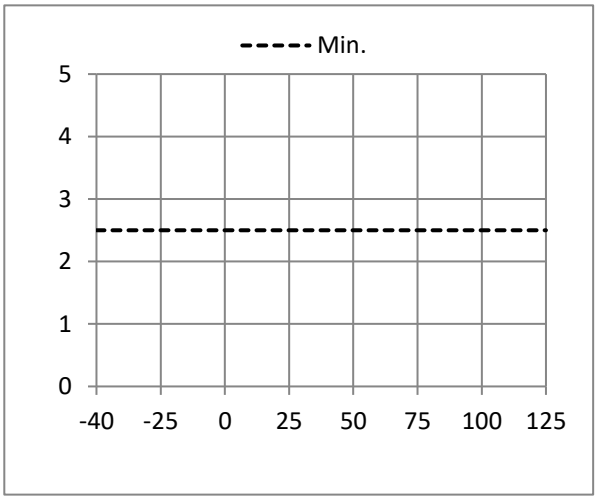


Figure 7B Logic “1” Input Voltage vs Temperature

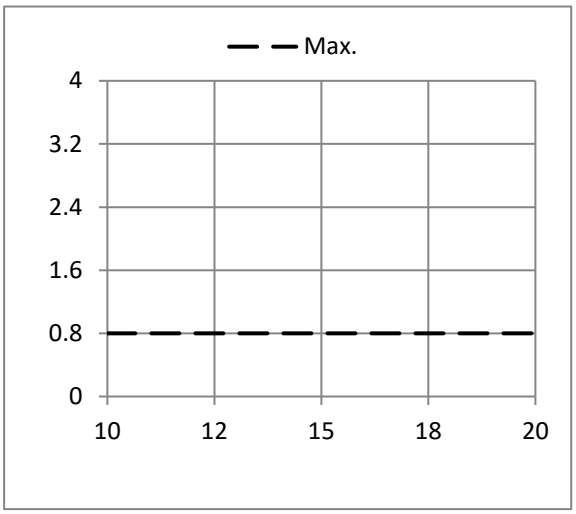


Figure 8A Logic “0” Input Voltage vs Supply Voltage

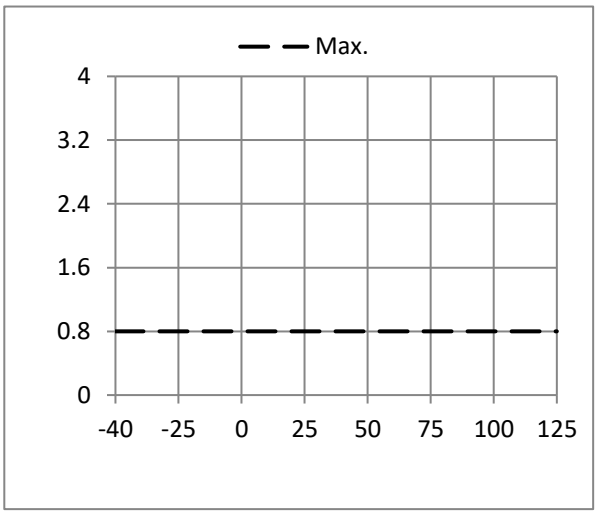


Figure 8B Logic “0” Input Voltage vs Temperature

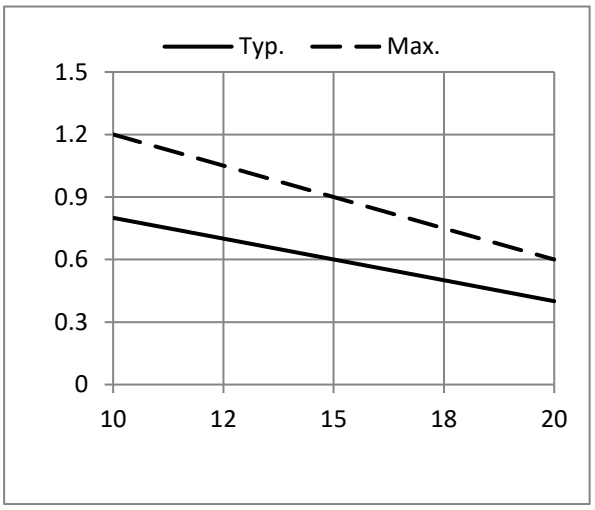


Figure 9A High-level Output Voltage vs Supply Voltage

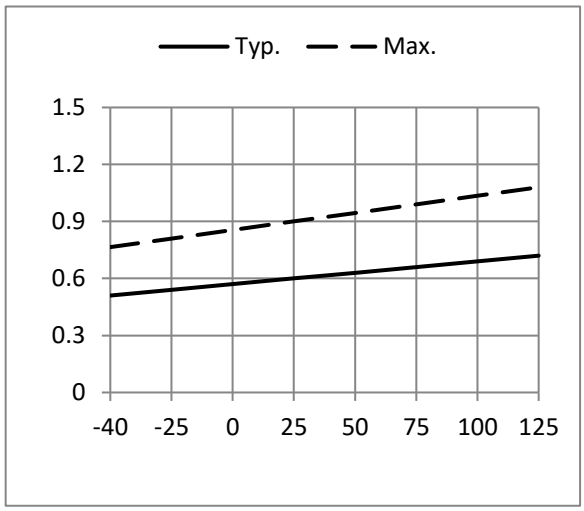


Figure 9B High-level Output Voltage vs Temperature

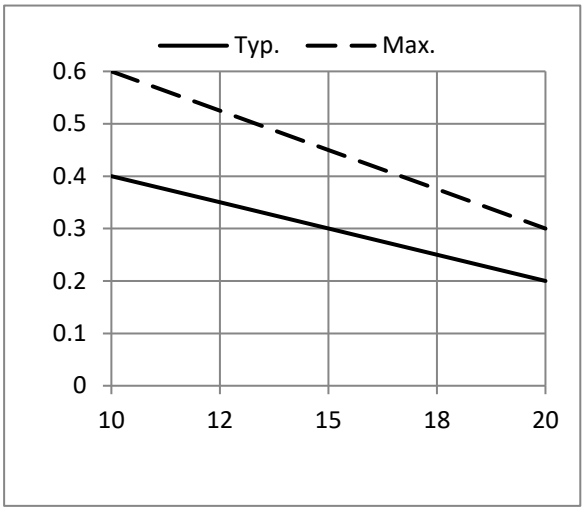


Figure 10A Low Level Output Voltage vs Supply Voltage

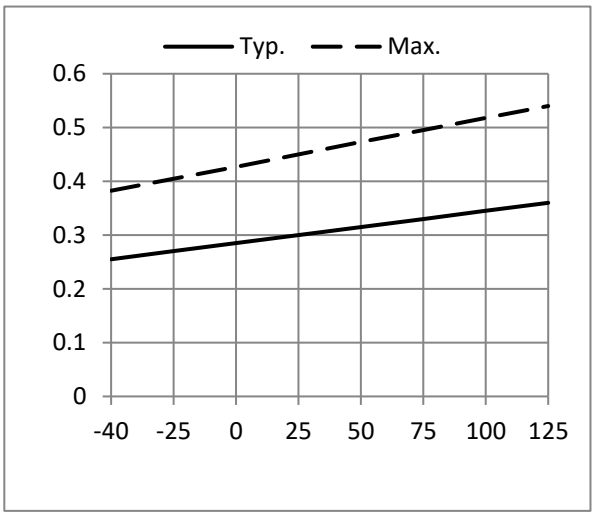


Figure 10B Low Level Output Voltage vs Temperature

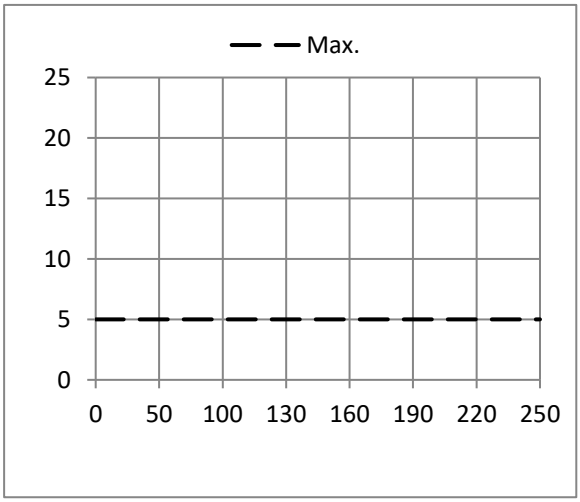


Figure 11A Offset Supply Current vs Voltage

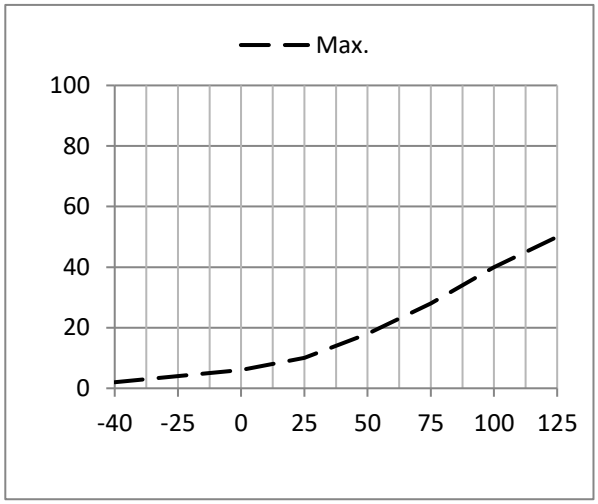


Figure 11B Offset Supply Current vs Temperature

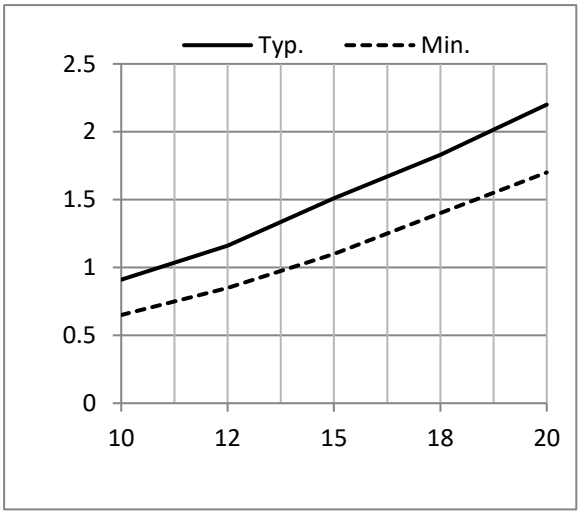


Figure 12A Output Source Current vs Supply Voltage

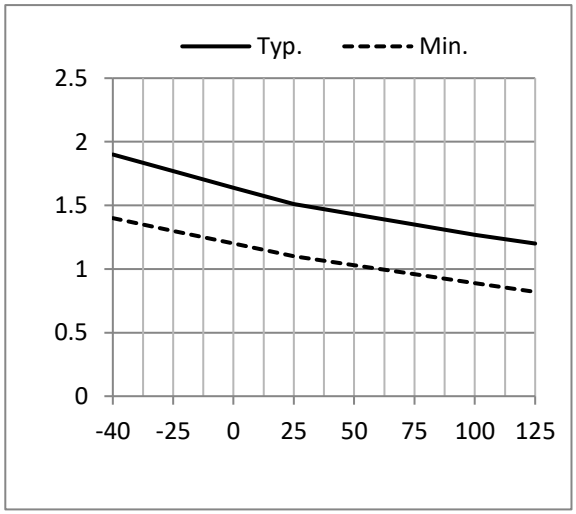


Figure 12B Output Source Current vs Temperature

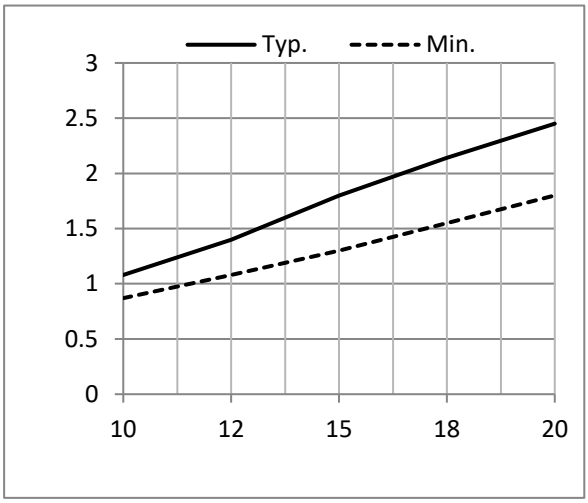


Figure 13A Output Sink Current vs Supply Voltage

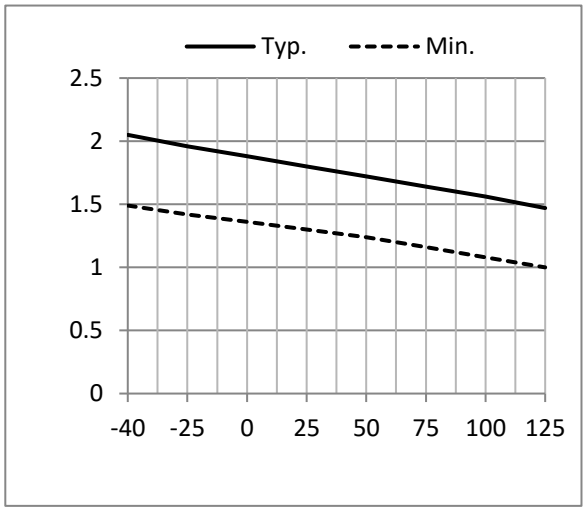


Figure 13B Output Sink Current vs Temperature

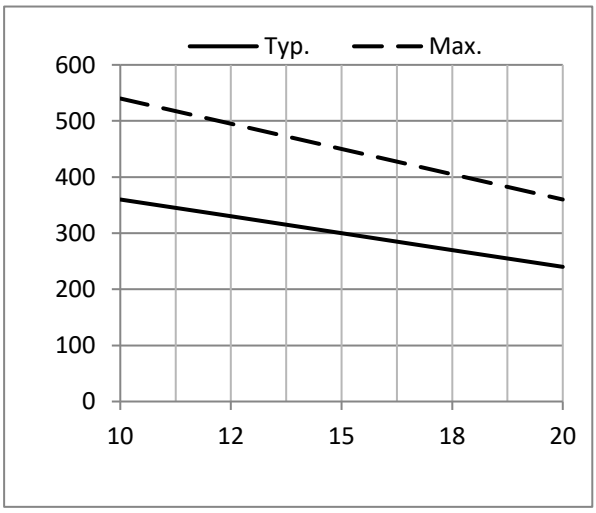


Figure 14A Turn On Time vs Supply Voltage

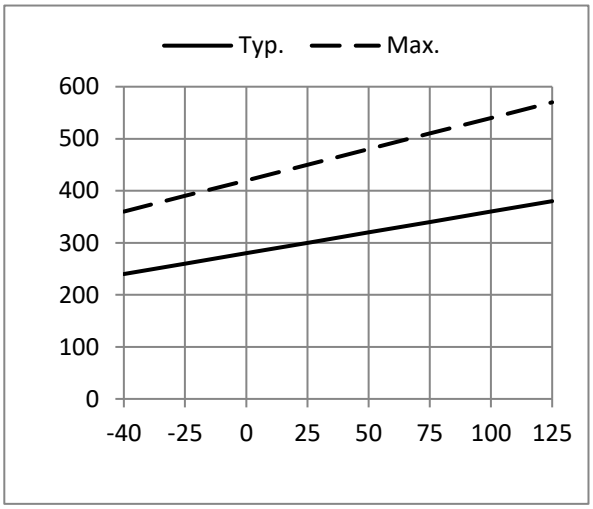


Figure 14B Turn On Time vs Temperature

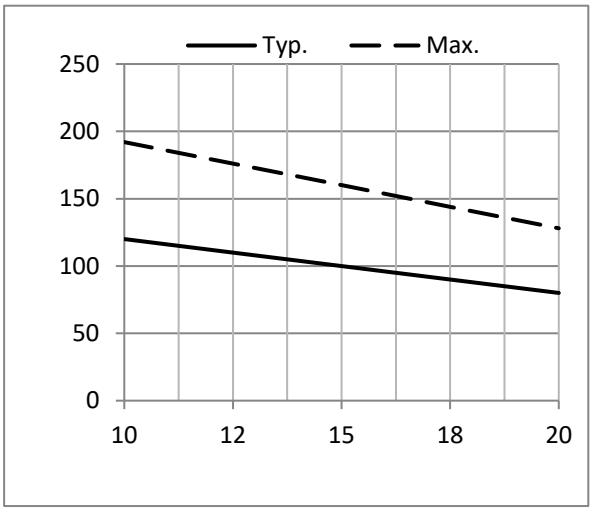


Figure 15A Turn Off Time vs Supply Voltage

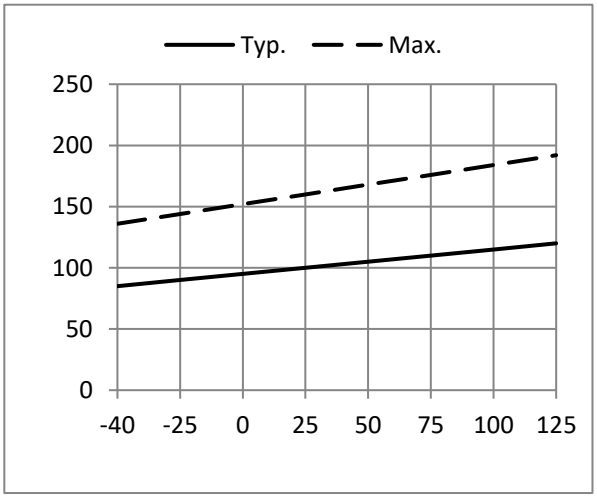


Figure 15B Turn Off Time vs Temperature

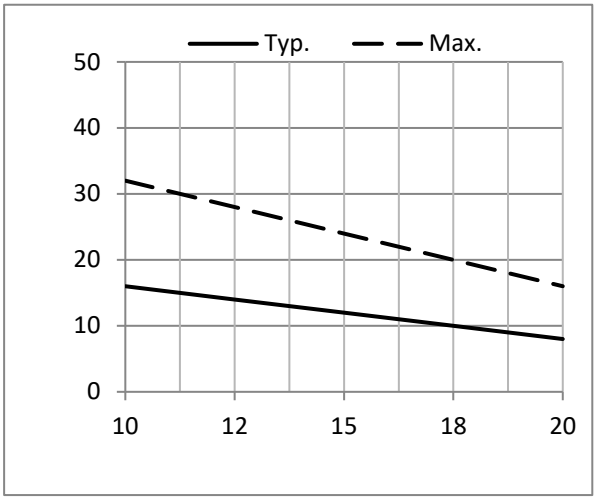


Figure16A Turn On Rise Time vs Supply Voltage

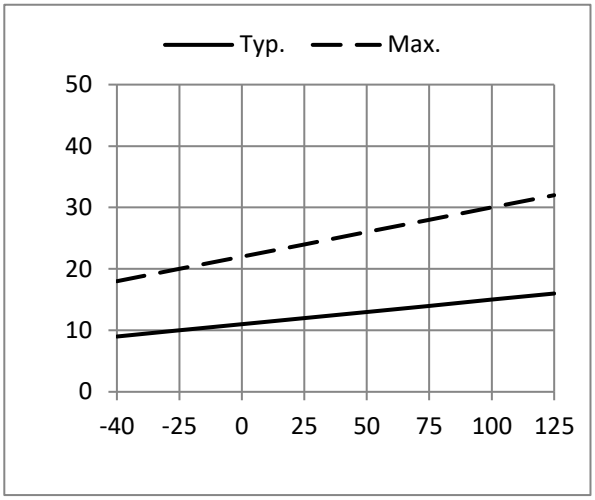


Figure 16B Turn On Rise Time vs Temperature

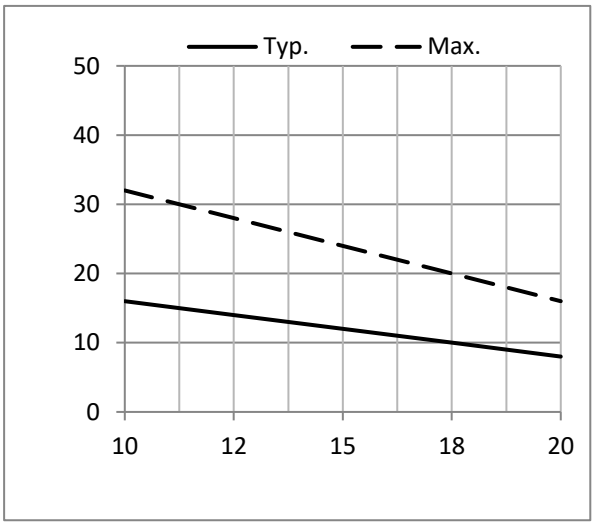


Figure 17A Turn Off Fall Time vs Supply Voltage

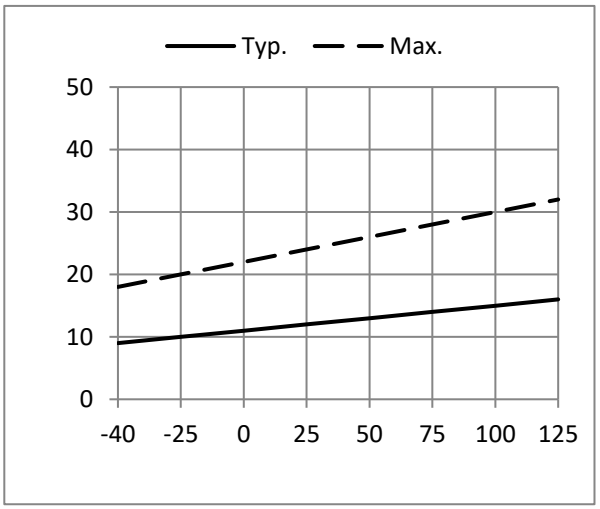


Figure 17B Turn Off Fall Time vs Temperature

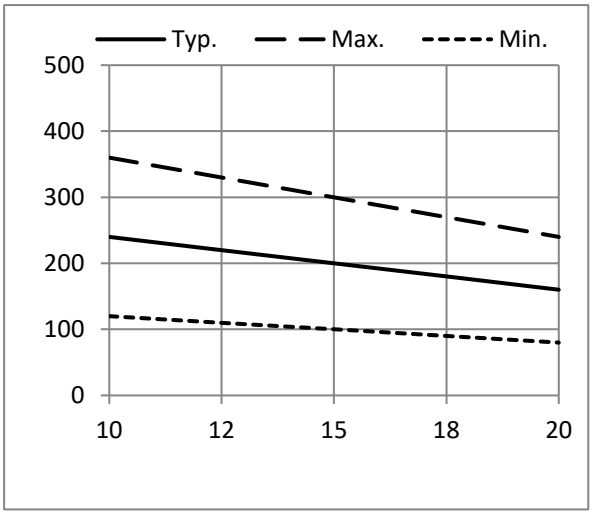


Figure 18A Dead Time vs Supply Voltage

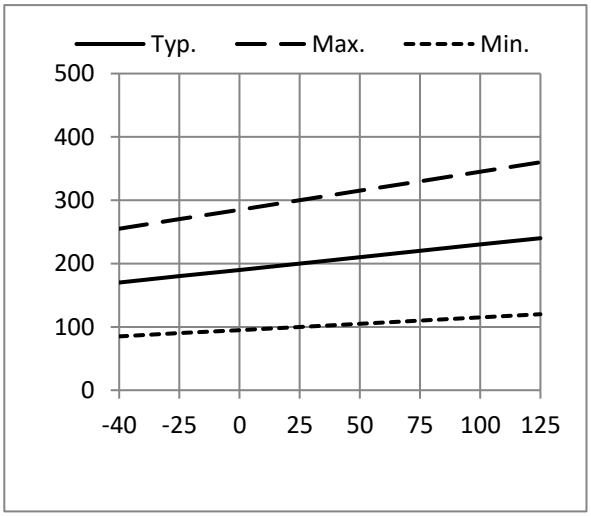


Figure 18B Deadtime Time vs Temperature

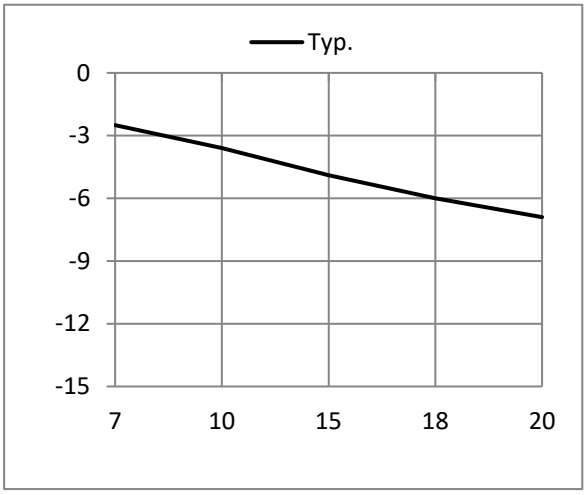


Figure 19A V_S Negative offset vs Supply Voltage

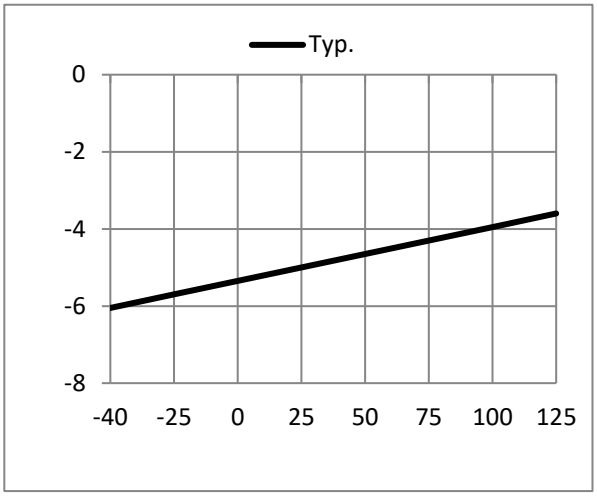


Figure 19B V_S Negative offset vs Temperature

8 Revision History

Rev.	Descriptions	Date	Prepared By
V1.0	First release.	2016/04/18	Raymond Xie
V1.1	Added product model and changed FD6288 to FD6288T&Q	2016/12/18	Raymond Xie
V1.2	Removed top-level silk prints and added packaging information.	2018/01/05	Raymond Xie
V1.3	Proofread some descriptions.	2019/01/22	Raymond Xie
V1.4	1. Corrected Typical Application Diagram; 2. Corrected some descriptions and word spellings; 3. Standardized document format.	2023/04/24	Lay Ye / Eric Deng

Copyright Notice

Right to make changes — Fortior Technology (Shenzhen) Co., Ltd. reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. The information contained in this manual is provided for the general use by our customers. Our customers should ensure that they take appropriate action so that their use of our products does not infringe upon any patents. It is the policy of Fortior Technology (Shenzhen) Co., Ltd. to respect the valid patent rights of third parties and not to infringe upon or assist others to infringe upon such rights.

If there are any differences between the Chinese and the English contents, please take the Chinese version as the standard.

Fortior Technology (Shenzhen) Co., Ltd.
Room 203, 2/F, Building No.11, Keji Central Road 2,
Software Park, High-Tech Industrial Park, Shenzhen, P.R. China 518057
Tel: 0755-26867710
Fax: 0755-26867715
URL: http://www.fortiortech.com