FD2607S

600V Half bridge gate driver

Description

FD2607S is a high voltage, high speed half bridge gate driver. It can drive N-type power MOSFETs and IGBTs

FD2607S has also built-in VCC undervoltage (UVLO) protection to prevent the power semiconductor devices from operation under very low voltage.

FD2607S has also built-in cross-conduction prevention logic protection and dead time. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction, and thus protect effectively the power devices.

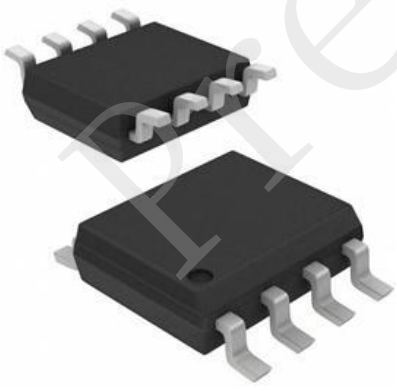
Features

- Suspension absolute voltage +600V
- Power supply pressure range: 10V ~20V
- 3.5V/5V input logic compatible
- VCC Undervoltage protection (UVLO)
- Output is in phase with the input
- Cross-conduction prevention logic
- Built-in dead time
- High and low channel matching
- RoHS compliant

Applications

- Motor drives
- DC-AC inverter drives

Packages



SOP8

1. Absolute Maximum Rating (All pins are referenced to COM unless otherwise stated)

Parameter	Symbol	Min~Max	Units
High side floating absolute voltage	V_B	-0.3～625	V
High side floating offset	V_S	V_B-25～V_B+0.3	V
High side output voltage	V_{HO}	V_S -0.3～V_B +0.3	V
Low side supply voltage	V_{CC}	-0.3～25	V
Low side output voltage	V_{LO}	-0.5～V_{CC}+0.3	V
Logic input voltage（HIN,LIN）	V_{IN}	-0.3～6.5	V
Offset voltage slew rate range	dV_S/dt	≤50	V/ns
Power dissipation @T_A≤25°C	P_D	≤0.625	W
Thermal resistance, junction to ambient	R_{thJA}	≤200	°C/W
Junction temperature	T_j	≤150	°C
Storage temperature	T_{stg}	-55～150	°C

Note1: In any case, power dissipation should not exceed P_D.

Note2: Voltages above the absolute maximum ratings may damage the chip.

2. Recommended Operating Conditions (All voltages are referenced to COM)

Definition	Symbol	Min	Max	Units
High-side float absolute voltage	V_B	V_S+10	V_S+20	V
High-side floating offset voltage	V_S	Note1	600	V
High-side output voltage	V_{HO}	V_S	V_B	V
Low-side supply voltage	V_{CC}	10	20	V
Low side output voltage	V_{LO}	0	V_{CC}	V
Logic input voltage（HIN, LIN）	V_{IN}	0	5.5	V
Environment temperature	T_A	-40	125	°C

Note1: Logic operational for V_S of (COM – 5V) to (COM + 600V). Logic state held for V_S of (COM – 5V) to (COM –V_{BS}).

Note2: The long-term operation of the chip outside the recommended conditions may affect its reliability. It is not recommended to work in an environment that exceeds the recommended conditions.

3. Static Electrical Characteristics

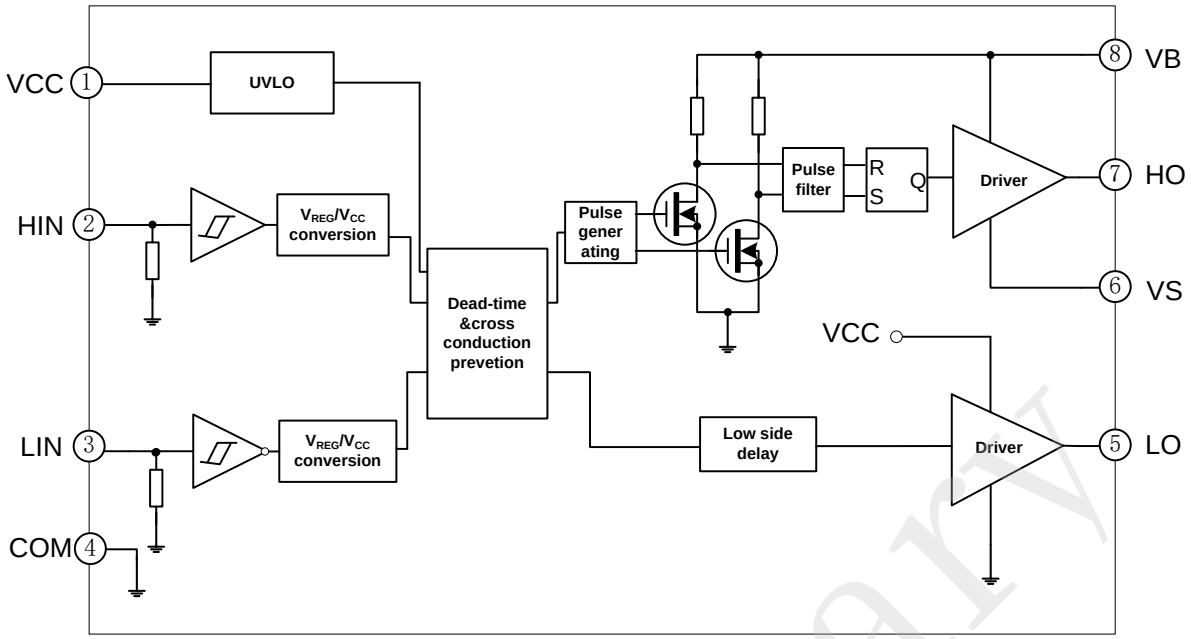
V_{BIAS} (V_{CC}, V_{BS}) =15V and TA =25°C unless otherwise specified. All the parameters are referenced to COM.

Definition	Symbol	Test conditions	Min.	Typ.	Max.	Units
Logic "1" input voltage	V_{IH}		2.7	-	-	V
Logic "0" input voltage	V_{IL}		-	-	0.8	
High level output voltage, V_{BIAS} - V_O	V_{OH}	I_O=20mA	-	0.7	1.20	
low level output voltage, V_O	V_{OL}		-	0.2	0.35	
Offset supply leakage current	I_{LK}	V_B =V_S =600V	-	1.0	5.0	uA
Quiescent V_{BS} supply current	I_{QBS}	V_{IN} =0V or 5V	-	50	90	
Quiescent V_{CC} supply current	I_{QCC}		-	210	380	
Logic "1" input bias current	I_{IN+}	V_{IN}=5V	-	25	50	
Logic "0" input bias current	I_{IN-}	V_{IN}=0V	-	-	1	
V_{CC} supply undervoltage positive going threshold	V_{CCUV+}		8.3	9.2	10.1	V
V_{CC} supply undervoltage negative going threshold	V_{CCUV-}		7.6	8.4	9.2	
V_{CC} Supply Under-Voltage Lock- Out Hysteresis	V_{CCUVH}		0.4	0.8	-	
Output high short circuit pulsed current	I_{O+}	V_O=0V,PW≤10us	140	250	-	mA
Output low short circuit pulsed current	I_{O-}	V_O=15V,PW≤10us	250	410	-	

4. Transient electrical parameters (T_A =25°C，V_{CC}=V_{BS}=15V，C_L=1000pF，V_S=COM, unless otherwise specified)

Parameter	Symbol	Condition for texting	Min	Typical	Max	Unit
Output rising edge transmission time	t_{on}	V_S=0V	--	90	160	ns
Output falling edge transmission time	t_{off}	V_S=600V	--	110	180	ns
High-low side delay match	MT		--	0	50	ns
Output rising time	t_r		--	85	130	ns
Output falling time	t_f		--	45	80	ns
Dead-time	DT		--	360	510	ns

5. Circuit diagram



6. Chip pin configuration

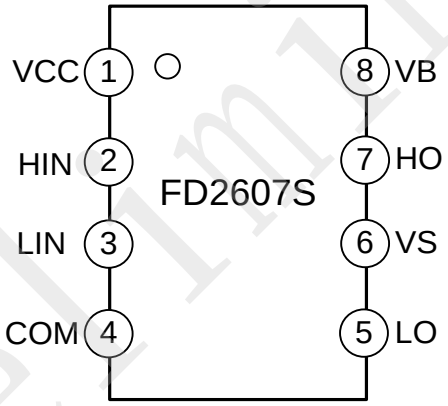
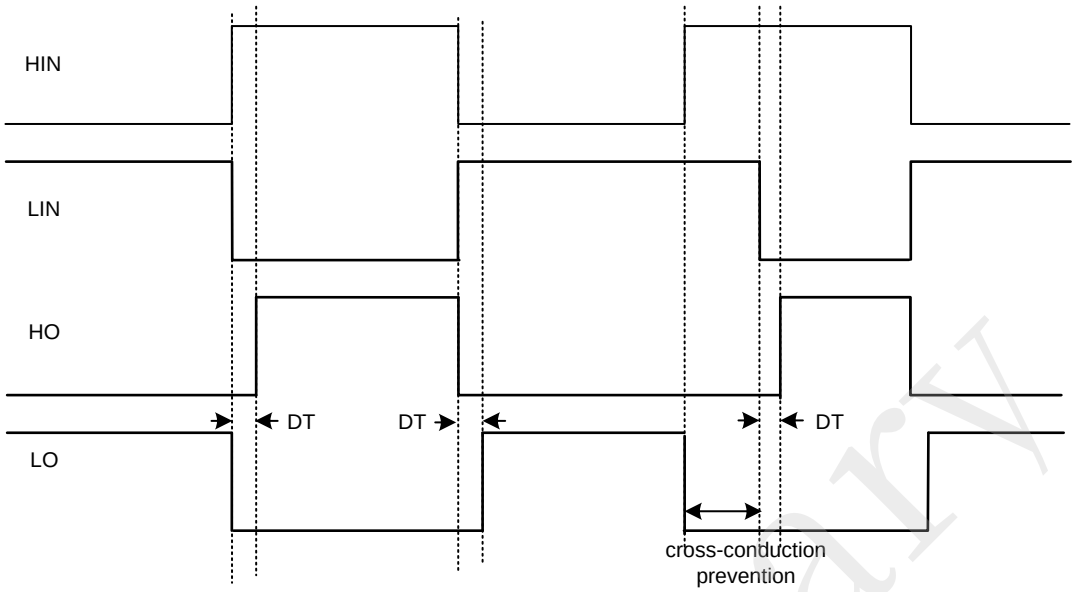


Figure 6-1 Package pin diagram

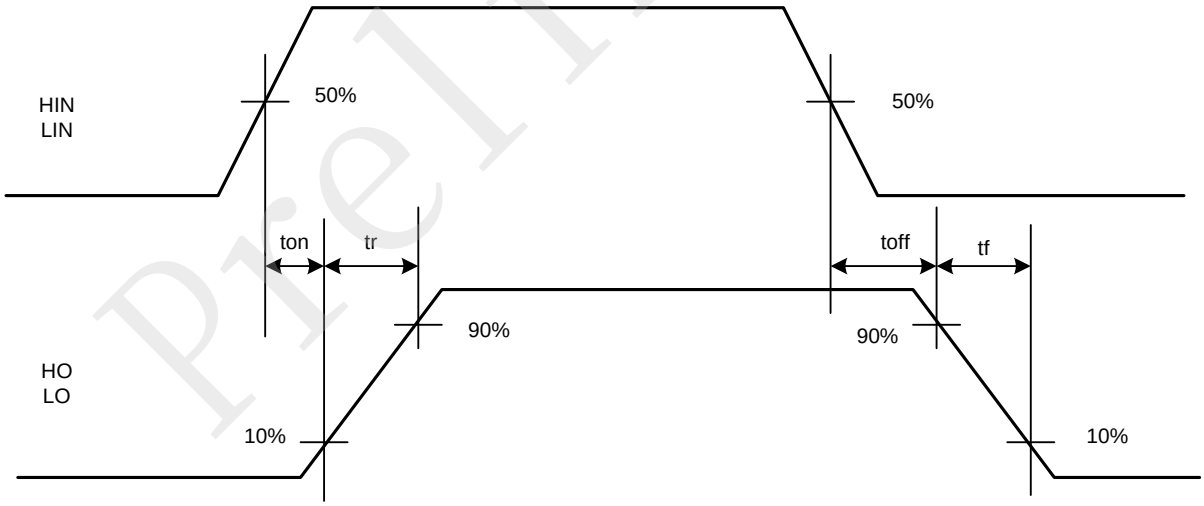
Table 6-1 Package pin

Pin no.	Pin name	Pin description
1	VCC	Low-side supply voltage
2	HIN	High-side input
3	LIN	Low-side input
4	COM	Ground
5	LO	Low-side output
6	VS	High-side floating offset voltage
7	HO	High-side output
8	VB	High-side float absolute voltage

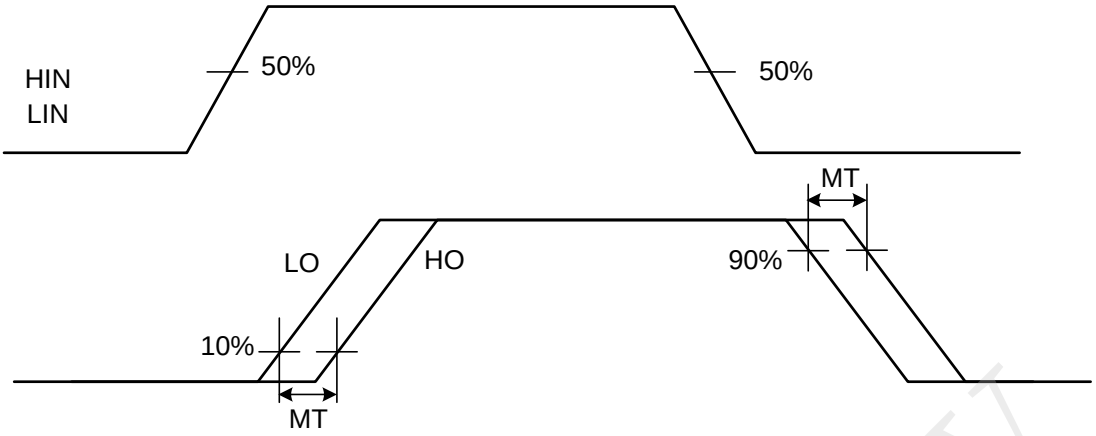
7. Logic timing diagram



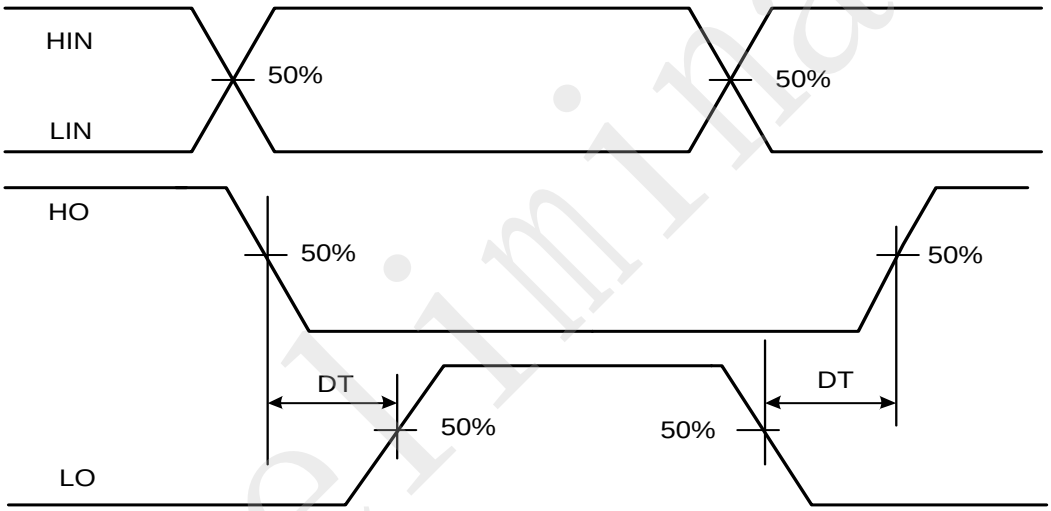
8. Switching time test standards



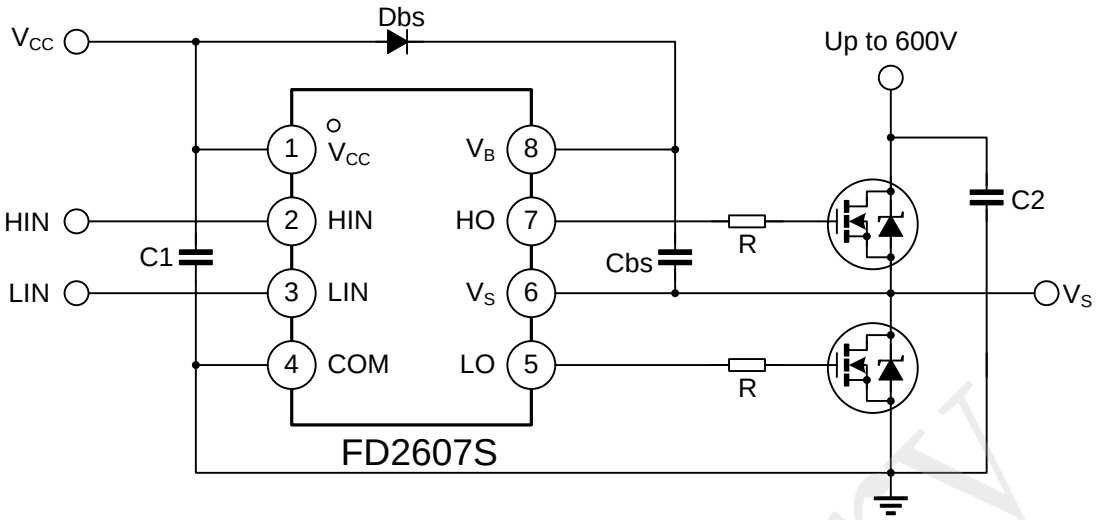
9. Transmission time matching test standards



10. Dead time test standards



11. Typical application circuit



C1： Power filter capacitor, according to the circuit can choose 1μF ~ 10μF, as close to the chip pin as possible.

R： Gate drive resistor, and the resistance depends on the device being driven.

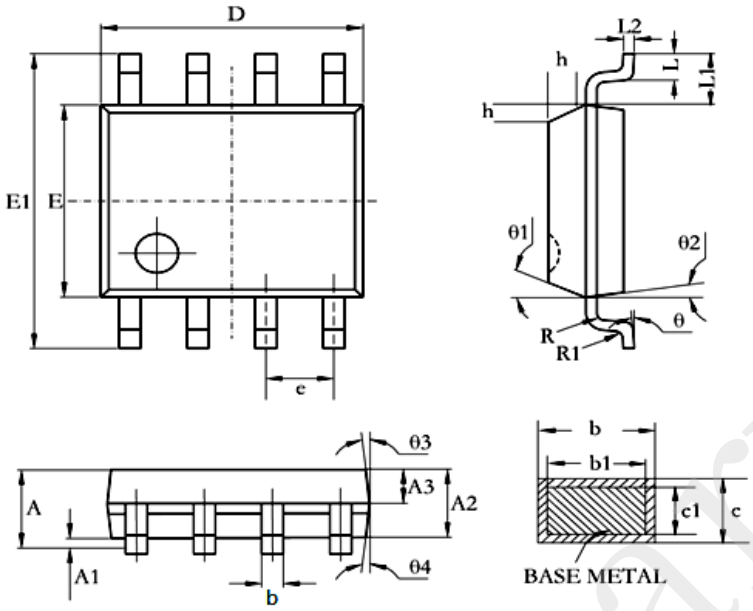
Dbs：Bootstrap diodes. It should be selected for high reverse breakdown voltage Schottky diodes.

Cbs：Bootstrap capacitors. Ceramic capacitors or tantalum capacitors should be selected, according to the circuit can choose 0.22μF ~ 10μF. The capacitor should be as close as possible to the chip pin.

Note:

The above circuits and parameters are for reference only. The actual application circuit should be designed with the measured results in setting the parameters.

12. Package size（SOIC-8）



Symbol	Dimensions in mm			Dimensions in inches		
	Min	Nom	Max	Min	Nom	Max
A	1.36	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.25	1.40	1.65	0.049	0.055	0.065
A3	0.50	0.60	0.70	0.020	0.024	0.028
b	0.38	-	0.51	0.015	-	0.020
b1	0.37	0.42	0.47	0.015	0.017	0.019
c	0.17	-	0.25	0.007	-	0.010
c1	0.17	0.20	0.23	0.007	0.008	0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	5.80	6.00	6.20	0.228	0.236	0.244
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC					
L	0.45	0.60	0.80	0.018	0.024	0.031
L1	1.04REF					
L2	0.25BSC					
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
h	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	-	8°	0°	-	8°
θ1	15°	17°	19°	15°	17°	19°
θ2	11°	13°	15°	11°	13°	15°
θ3	15°	17°	19°	15°	17°	19°
θ4	11°	13°	15°	11°	13°	15°

Product number	Package	Marking	Packing	Quantity
FD2607S	SOP8	FD2607S	Tape & Reel	3000

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