Datasheet

3-Phase BLDC Motor Controller with Built-in Pre-Driver FT8132

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FT8132 3-Phase BLDC Motor Controller with Built-in Pre-driver

1 System Introduction

1.1 Overview

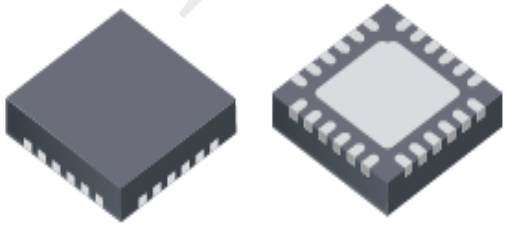
FT8132 is an IC with built-in 3-phase pre-driver designed for BLDC motor drive system. Thanks to the high integration, few peripheral is required. The chip control motor with advanced control performing reduced noise and vibration. GUI can configure motor parameters, startup control parameters and speed regulation mode which are stored in built-in EEPROM. Analog voltage, PWM, I2C interface or CLOCK mode is optional for motor speed regulation. The speed indication function is integrated, which could indicate motor speed in real time through FG pin or I2C interface. Speed control mode, current control mode, power control mode or voltage control mode is optional. The protection against overcurrent, undervoltage, overvoltage, external overtemperature, lock, phase loss and Hall error is integrated to ensure the safe operation of motor. The sleep current of chip is about 60μA.

1.2 Applications

Floor fans, cooling fans, ceiling fans, robot vacuum and vacuum cleaners.

1.3 Features

- Sensorless FOC mode
- Hall effected SVPWM (Hall IC/ sensor) mode
- Hall effected FOC mode (Hall IC/ sensor)
- 3P3N Pre-driver with configurable deadtime
- Speed control mode, current control mode, power control mode or voltage control mode
- Analog voltage, PWM, I2C interface or CLOCK mode for motor speed regulation
- Real time information interactions by I2C for motor control and motor states readback
- Rotor initial position detection
- Tail wind and contrary wind detection
- Soft-On, Soft-Off
- Built-in EEPROM
- Configurable multi-segment output curve
- Protection of overcurrent, undervoltage, overvoltage, external overtemperature, lock, phase loss and Hall error
- Forward or reverse rotation direction selectable
- FG and RD output



QFN24

SSOP24

1.4 Typical Application Diagram

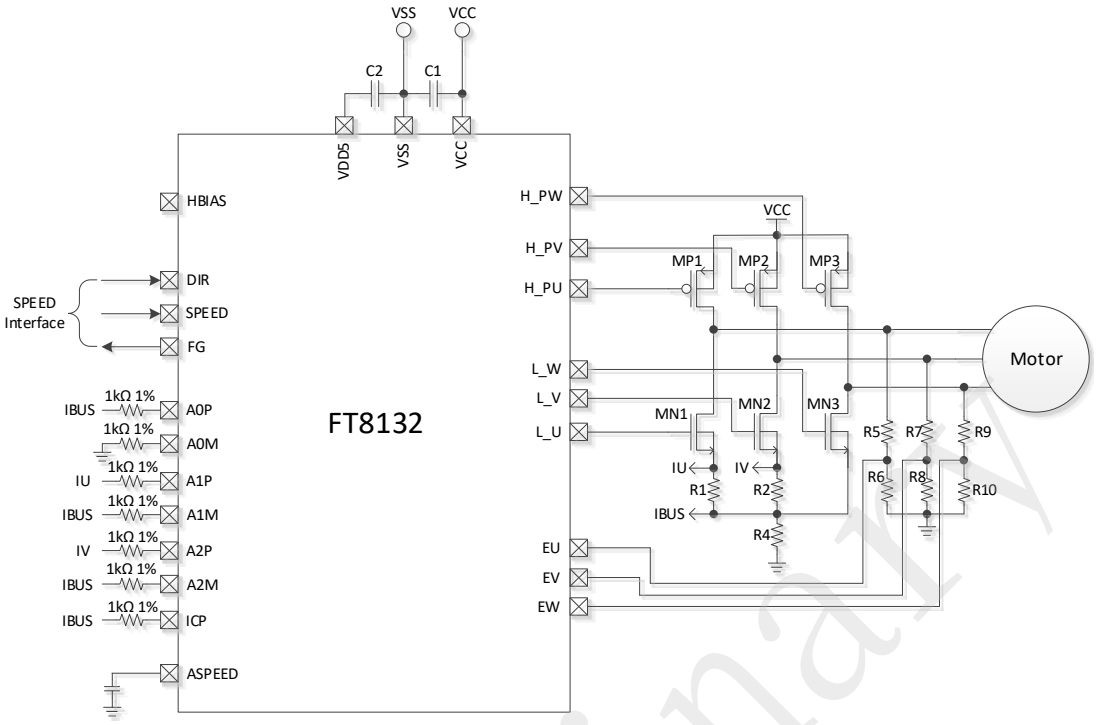


Figure 1-1 Typical Application Diagram of Dual-Resistance Sampling Sensorless FOC based Drive System

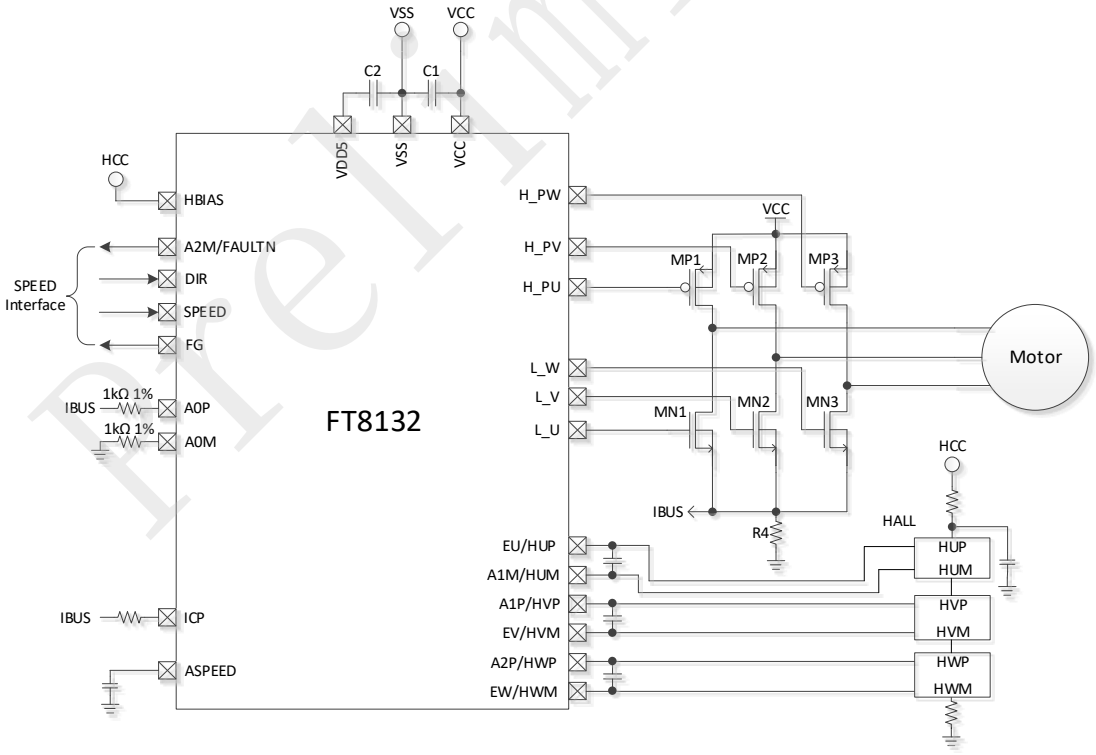


Figure 1-2 Typical Application Diagram of Single-Resistance Sampling Hall-Sensor based Drive System

1.5 Functional Block Diagram

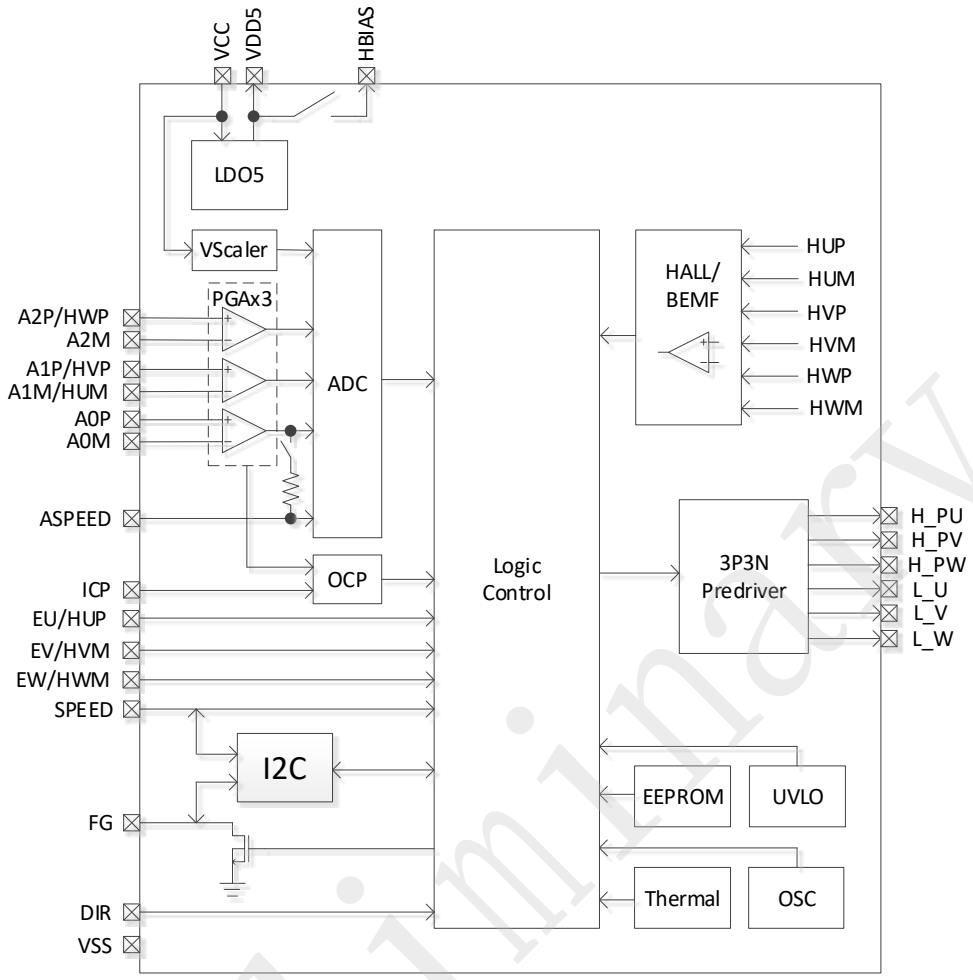


Figure 1-3 Functional Block Diagram of FT8132 with Sensorless Control

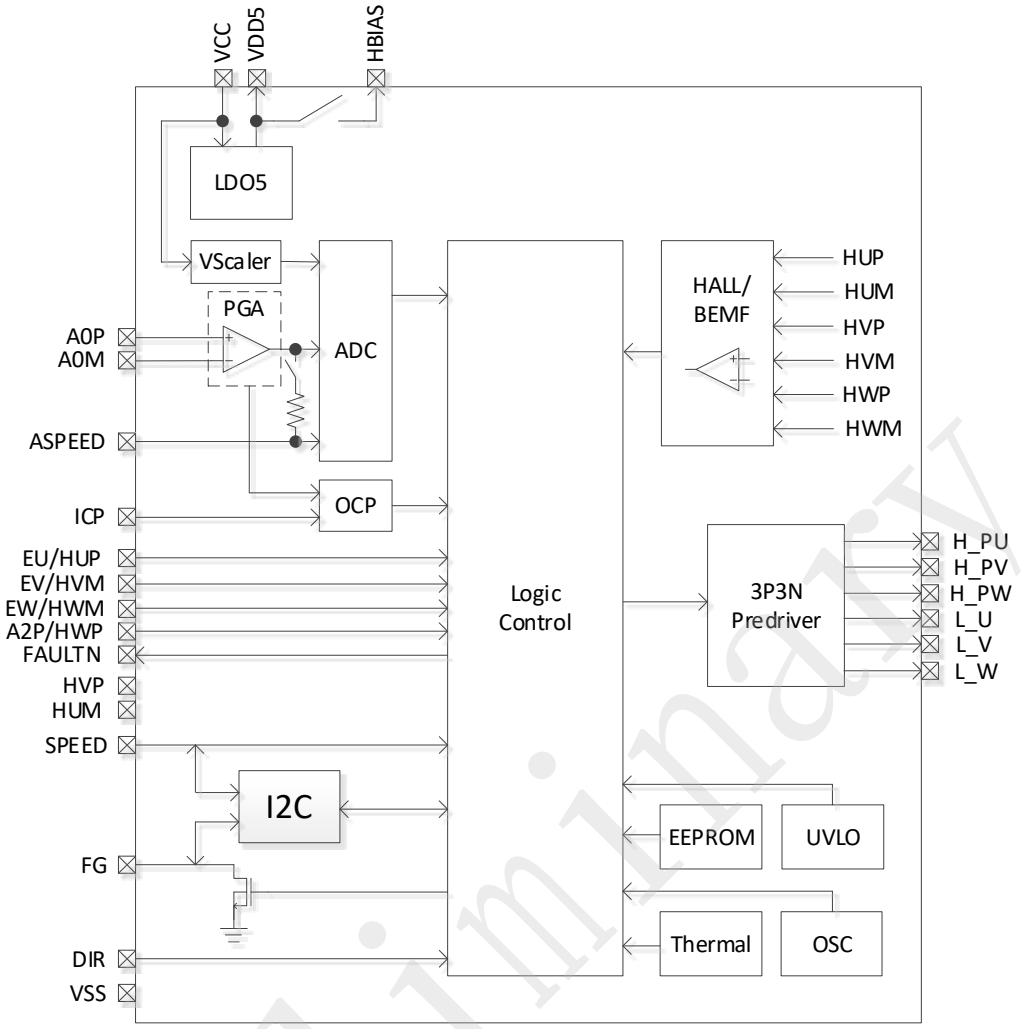


Figure 1-4 Functional Block Diagram of FT8132 with Hall Effected Control

1.6 Pinout

1.6.1 Pinout of FT8132Q QFN24

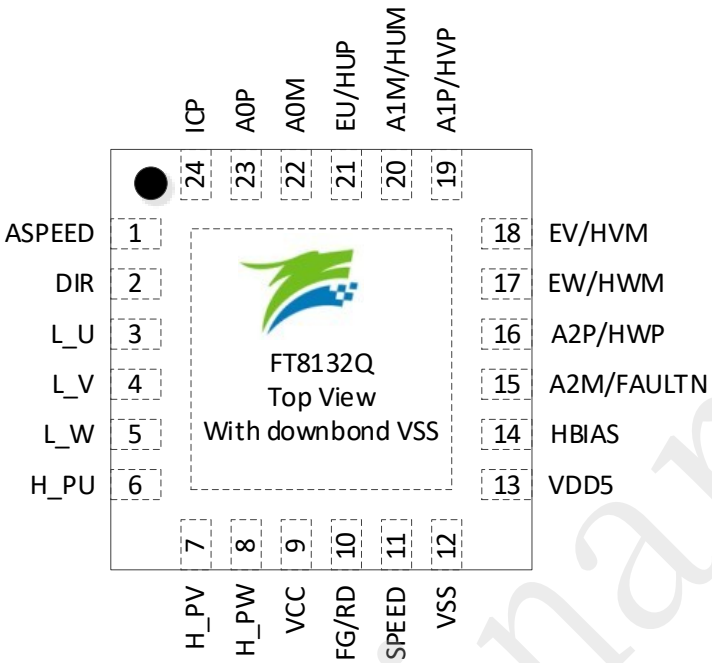


Figure 1-5 Pinout of FT8132 QFN24

1.6.2 Pinout of FT8132S SSOP24

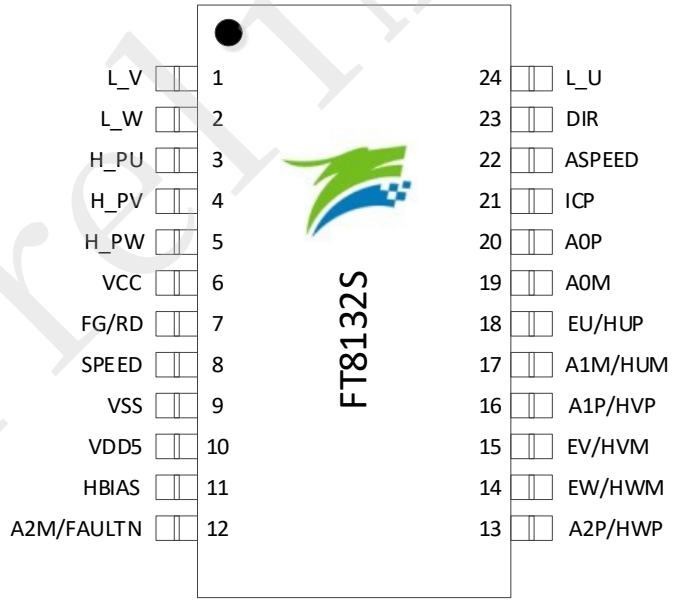


Figure 1-6 Pinout of FT8132 SSOP24

1.7 Pin Definition

1.7.1 FT8132Q QFN24 Pin List

Table 1-1 FT8132 QFN24 Pin List

Pin	FT8132 QFN24	IO Type	Description
ASPEED	1	AI	Input of analog voltage speed regulation mode
DIR	2	DI	Motor rotation direction selection with built-in pull-up resistance 0: Reverse rotation. The output phase sequence is UWV 1: Forward rotation. The output phase sequence is UVW
L_U	3	DO	3P3N pre-driver U phase low side output
L_V	4	DO	3P3N pre-driver V phase low side output
L_W	5	DO	3P3N pre-driver W phase low side output
H_PU	6	DO	3P3N pre-driver U phase high side output
H_PV	7	DO	3P3N pre-driver V phase high side output
H_PW	8	DO	3P3N pre-driver W phase high side output
VCC	9	P	Power supply. The input voltage range is 6V ~ 28V. Shunt a more than 10μF capacitance to ground
FG/RD	10	DO	Motor speed or lock state signal, with collector open-drain output
SPEED	11	DI	Input of PWM or CLOCK mode based speed regulation
VSS	12	P	Ground
VDD5	13	P	The output of internal LDO and the voltage is 5V. Shunt a 1μF ~ 4.7μF capacitance to ground
HBIAS	14	DO	Hall bias power supply, internally connected to VDD5 through a configurable switch
A2M/ FAULTN	15	AI/ DO	Negative input of AMP2 Fault output signal, with collector open-drain output
A2P/ HWP	16	AI/ AI	Positive input of AMP2 Positive input of W phase Hall-sensor
EW/ HWM	17	AI/ AI	W phase BEMF input after resistor division Negative input of W phase Hall-sensor or input of W phase Hall-IC
EV/ HVM	18	AI/ AI	V phase BEMF input after resistor division Negative input of V phase Hall-sensor or input of V phase Hall-IC
A1P/ HVP	19	AI/ AI	Positive input of APM1 Positive input of V phase Hall-sensor
A1M/ HUM	20	AI/ AI	Negative input of APM1 Negative input of U phase Hall-sensor
EU/ HUP	21	AI/ AI	U phase BEMF input after resistor division Positive input of U phase Hall-sensor or input of U phase Hall-IC
A0M	22	AI	Negative input of APM0
A0P	23	AI	Positive input of APM0
ICP	24	AI	Input of overcurrent protection

Notes:

- DI = Digital Input
- DO = Digital Output
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

1.7.2 FT8132S SSOP24 Pin List

Table 1-2 FT8132 SSOP24 Pin List

Pin	FT8132S SSOP24	IO Type	Description
L_V	1	DO	3P3N pre-driver V phase low side output
L_W	2	DO	3P3N pre-driver W phase low side output
H_PU	3	DO	3P3N pre-driver U phase high side output
H_PV	4	DO	3P3N pre-driver V phase high side output
H_PW	5	DO	3P3N pre-driver W phase high side output
VCC	6	P	Power supply. The input voltage range is 6V ~ 28V. Shunt a more than 10μF capacitance to ground
FG/RD	7	DO	Motor speed or lock state signal, with collector open-drain output
SPEED	8	DI	Input of PWM or CLOCK mode based speed regulation
VSS	9	P	Ground
VDD5	10	P	The output of internal LDO and the voltage is 5V. Shunt a 1μF ~ 4.7μF capacitance to ground
HBIAS	11	DO	Hall bias power supply, internally connected to VDD5 through a configurable switch
A2M/ FAULTN	12	AI/ DO	Negative input of AMP2 Fault output signal, with collector open-drain output
A2P/ HWP	13	AI/ AI	Positive input of AMP2 Positive input of W phase Hall-sensor
EW/ HWM	14	AI/ AI	W phase BEMF input after resistor division Negative input of W phase Hall-sensor or input of W phase Hall-IC
EV/ HVM	15	AI/ AI	V phase BEMF input after resistor division Negative input of V phase Hall-sensor or input of V phase Hall-IC
A1P/ HVP	16	AI/ AI	Positive input of APM1 Positive input of V phase Hall-sensor
A1M/ HUM	17	AI/ AI	Negative input of APM1 Negative input of U phase Hall-sensor
EU/ HUP	18	AI/ AI	U phase BEMF input after resistor division Positive input of U phase Hall-sensor or input of U phase Hall-IC
A0M	19	AI	Negative input of AMP0
A0P	20	AI	Positive input of AMP0
ICP	21	AI	Input of overcurrent protection
ASPEED	22	AI	Input of analog voltage speed regulation mode
DIR	23	DI	Motor rotation direction selection with built-in pull-up resistance 0: Reverse rotation. The output phase sequence is UWV 1: Forward rotation. The output phase sequence is UVW
L_U	24	DO	3P3N pre-driver U phase low side output

Notes:

- DI = Digital Input

- DO = Digital Output
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

2 Package

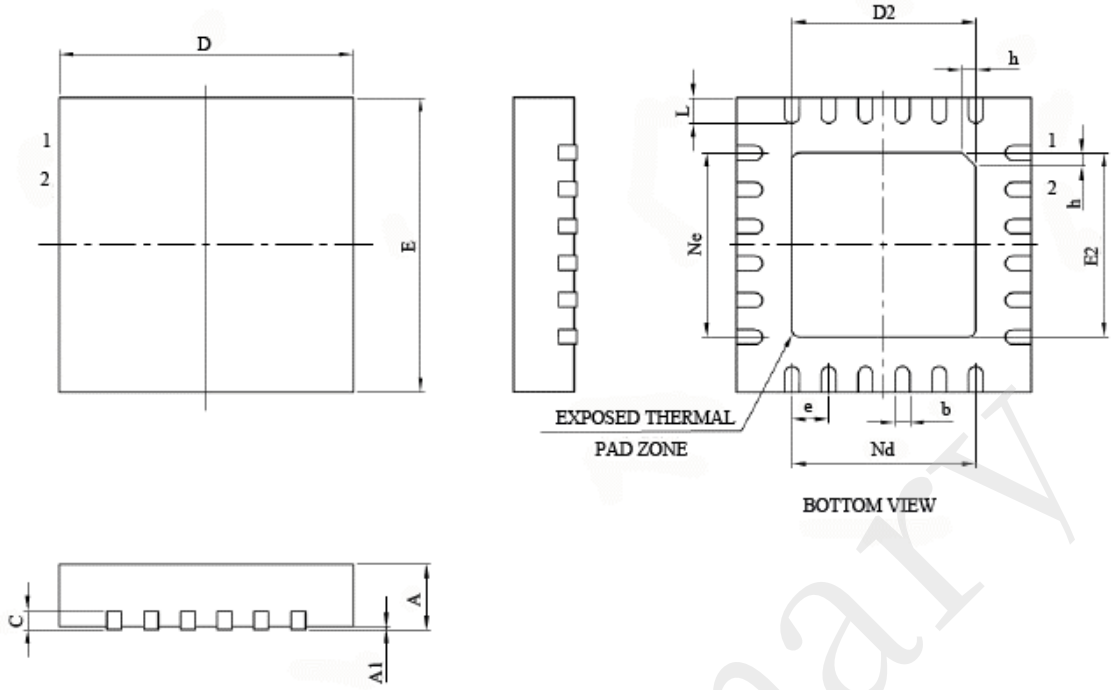


Figure 2-1 Package Size Diagram of QFN24

Table 2-1 Package Size Table of QFN24

Symbol	Dimensions In Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.35	2.50	2.65
L	0.35	0.40	0.45
h	0.30	0.35	0.40
N	Pin Number = 24		

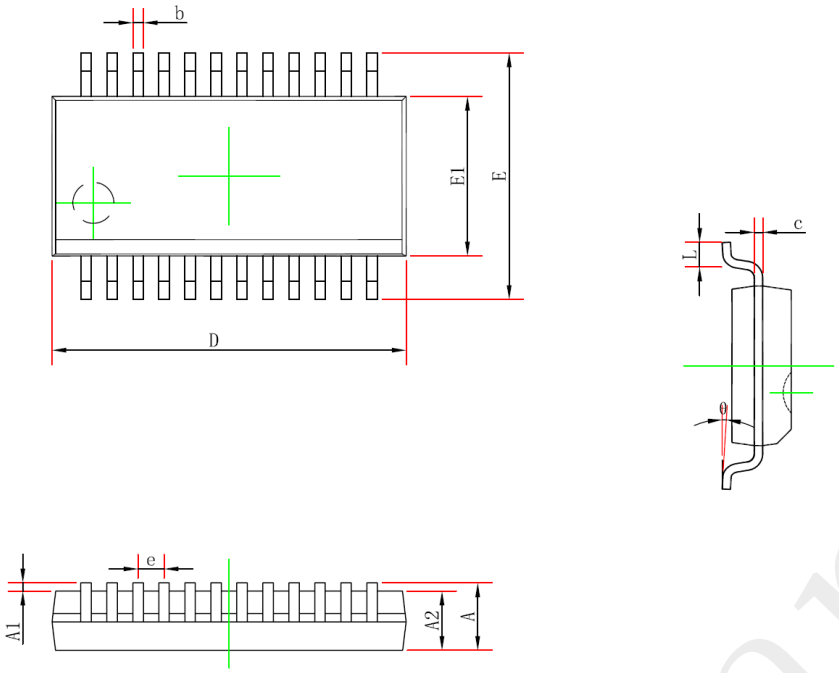


Figure 2-2 Package Size Diagram of SSOP24

Table 2-2 Package Size Table of SSOP24

Symbol	Dimensions In Millimeter		Dimensions In Inches	
	Min	Max	Min	Max
A	—	1.750	—	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	—	0.049	—
b	0.203	0.305	0.008	0.012
c	0.102	0.254	0.004	0.010
D	8.450	8.850	0.333	0.348
E1	3.800	4.000	0.150	0.157
E	5.800	6.200	0.228	0.244
e	0.635(BSC)		0.025(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

3 Ordering Information

Table 3-1 Package Type Information

Type	Package	Power Supply (V)	Driver Module	Control Functions						Protection							Operation Temperature T_j (°C)	Leadfree
				Driver Method	Speed Regulation Mode			Forward and Reverse Rotation	Initial Position Detection	Overcurrent Protection	Overtemperature Protection	Undervoltage Protection	Overvoltage Protection	Lock Protection	Hall Error Protection	Phase Loss Protection		
					I2C	PWM/ CLOCK	Analog Input											
FT8132Q	QFN24 (4x4mm)	6 ~ 28	3P3N Pre-driver	Hall effected & sensorless FOC	√	√	√	√	√	√	√	√	√	√	√	√	–40 ~ 150	√
FT8132S	SSOP24 (8.65x3.9mm)	6 ~ 28	3P3N Pre-driver	Hall effected & sensorless FOC	√	√	√	√	√	√	√	√	√	√	√	√	–40 ~ 150	√

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Operating junction temperature T_j		–40	—	150	℃
Storage temperature Tstg		–55	—	150	℃
VCC to VSS		–0.3	—	30	V
VDD5 to VSS		–0.3	5	6.5	V
FG to VSS		–0.3	—	VCC + 0.3	V
H_PU/H_PV/H_PW to VSS		–0.3	—	VCC + 0.3	V
L_U/L_V/L_W to VSS		–0.3	—	VCC + 0.3	V
DIR/ASPEED/ICP/A0P/A0M/ EU/A1M/A1P/EV/EW/A2P/ A2M/HBIAS/SPEED to VSS		–0.3	—	VDD5 + 0.3	V

Note: Exceeding the values listed in Table 4-1 may permanently damage the chip. These are stress ratings only, and functional operation of the device at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4.2 Global Electrical Characteristics

Table 4-2 Global Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
VCC operating voltage		6	—	28	V
VDD5 operating voltage	T_A = –40℃ ~ 85℃	4.8	5	5.2	V
VCC operating current I_{VCC}	T_A = –40℃ ~ 85℃	—	15	25	mA
VDD5 load current	T_A = –40℃ ~ 85℃	—	—	10	mA
VCC sleep current $I_{VCC\text{-}sleep}$	T_A = –40℃ ~ 85℃	—	50	100	μA

4.3 Protection Electrical Characteristics

Table 4-3 Protection Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
VCC hardware undervoltage threshold V_{UVLO}		4.8	5.4	6	V
VCC hardware undervoltage recover hysteresis $V_{UVLO-HYS}$		—	0.4	—	V
Junction temperature T_{TSD}	T_j is configured as 135℃	129	135	141	℃
Temperature hysteresis T_{TSD_HYS}		—	10	—	℃

4.4 IO Electrical Characteristics (DIR/SPEED/FG)

Table 4-4 IO Electrical Characteristics (DIR/SPEED/FG)

Parameter	Conditions	Min	Typ	Max	Unit
High level input voltage V_{IH}		0.6*VDD5	—	—	V
Low level input voltage V_{IL}		—	—	0.2*VDD5	V
SPEED/DIR/A1P pull-up resistor		—	33	—	kΩ
SPEED pull-down resistor		—	30	—	kΩ
EW/EV/EU/A2P/A2M pull-up resistor		—	5.6	—	kΩ

4.5 PWM/CLOCK Input Frequency Range

Table 4-5 PWM/CLOCK Input Frequency Range

Parameter	Conditions	Min	Typ	Max	Unit
PWM Input Frequency Range		100	—	100k	Hz
CLOCK Input Frequency Range		20	—	1400	Hz

4.6 Pre-driver Electrical Characteristics

Table 4-6 Pre-driver Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
High side output source current		—	150	—	mA
High side output sink current		—	90	—	mA
Low side output source current		—	150	—	mA
Low side output sink current		—	180	—	mA
Rising time of high side output	1nF Load, from 10% to 90%	—	25	—	ns
Falling time of high side output	1nF Load, from 90% to 10%	—	90	—	ns
Rising time of low side output	1nF Load, from 10% to 90%	—	115	—	ns
Falling time of low side output	1nF Load, from 90% to 10%	—	60	—	ns

4.7 ASPEED Electrical Characteristics

Table 4-7 ASPEED Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
ASPEED input voltage range		0	—	VDD5	V

4.8 Thermal Characteristics

Table 4-8 QFN24 Thermal Characteristics

Parameter	Conditions	Value	Unit
θ_{JA} Thermal resistance junction to ambient [1]	JEDEC standard, 2S2P PCB	50	°C/W
θ_{JC} Thermal resistance junction to case [1]	JEDEC standard, 2S2P PCB	25	°C/W

Note:

[1] Test results may vary depending on the actual conditions

Table 4-9 SSOP24 Thermal Characteristics

Parameter	Conditions	Value	Unit
θ_{JA} Thermal resistance junction to ambient [1]	JEDEC standard, 2S2P PCB	85	°C/W

Note:

[1] Test results may vary depending on the actual conditions

5 Function Description

5.1 VDD5

VDD5 is voltage reference and power supply of internal digital logic and analog circuits. VDD5 is unavailable for external circuits. Shunt a more than 1μF capacitance to ground to stabilize the power supply.

5.2 DIR

DIR is forward and reverse rotation selection pin and used to control the rotation direction of motor. The pin is internal pull-up and high level by default.

5.3 ICP

ICP is the input of sampling current when overcurrent protection is enabled.

5.4 ASPEED

ASPEED is the analog input of analog voltage speed regulation mode. When analog speed regulation is enabled, speed reference is controlled by the input of ASPEED.

5.5 SPEED

SPEED is the input of PWM/CLOCK speed regulation mode. The input signal is duty cycle (PWM mode) or frequency (CLOCK mode). SPEED is multiplexed as SCL of I2C.

5.6 FG

FG is the speed and fault state indication pin, with open drain output. When speed indication is enabled, FG outputs speed signal. When fault states indication is enabled, FG outputs high level voltage to show fault state of motor. FG is multiplexed as SDA of I2C.

5.7 HBIAS

HBIAS is Hall bias power supply which is internally connected to VDD5 through a configurable switch. The maximum load capacity is 10mA.

5.8 Speed Regulation

5.8.1 Speed Regulation Mode

Analog voltage, PWM, I2C interface or CLOCK mode is optional for speed regulation. Simultaneously, only one speed regulation can be enabled. The input of analog voltage mode is ASPEED. The input of PWM or CLOCK mode is SPEED. When I2C interface mode is enabled, SPEED is multiplexed as SCl and FG is multiplexed as SDA.

5.8.2 Speed Regulation Curve

The speed regulation curve of input and output is shown in the following figures. The value of X-axis is the input PWM duty cycle (the input of I2C or analog voltage can be converted into the corresponding PWM duty cycle). The value of Y-axis is output and represents different control reference under different motor control modes.

When voltage loop is selected as the motor control mode, the value of Y-axis represents the output voltage duty cycle. Multi segment output curve is available and composed by 5 configurable output reference points. The start duty cycle X_ON is configurable, and the maximum duty cycle PWM_X98 can be configured as 98% or 100%. There are 3 inflection points of speed regulation curve fixed at 25%, 50% and 75%. The corresponding output reference Y_ON, Y_25, Y_50, Y_75 and Y_MAX are configurable.

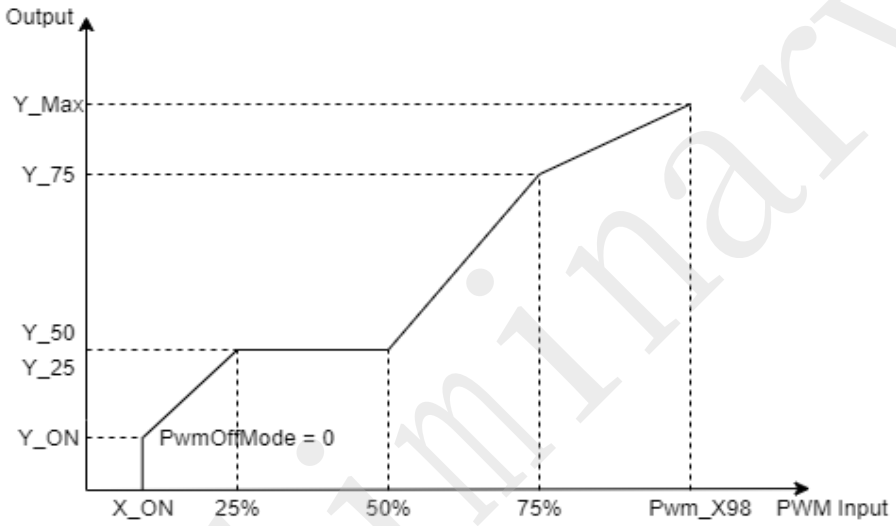


Figure 5-1 Multi Segment Output Curve in Voltage Control Mode (PwmOffMode = 0)

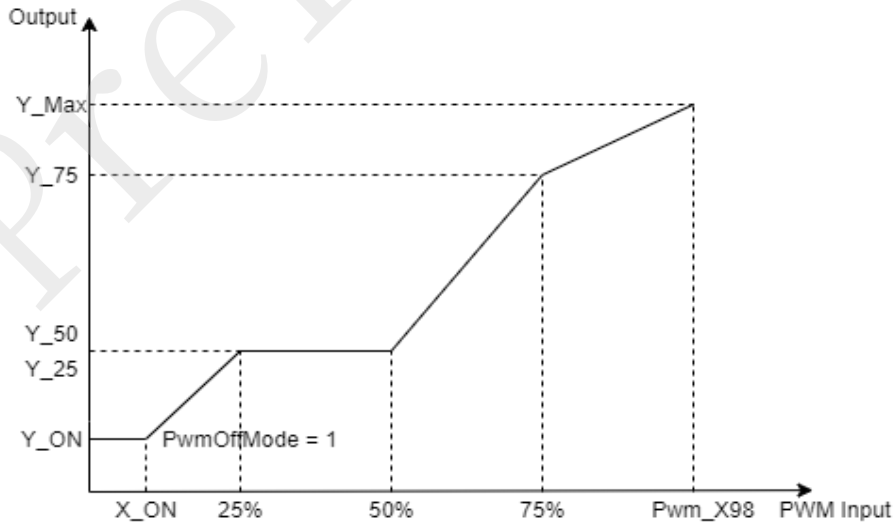


Figure 5-2 Multi Segment Output Curve in Voltage Control Mode (PwmOffMode = 1)

When the motor control mode is selected as speed control/current control/power control, the value of Y-axis represents motor speed/current/power. Multi segment output curve is unavailable and only Y_ON and Y_MAX are configurable. The output increases linearly with the change of input.

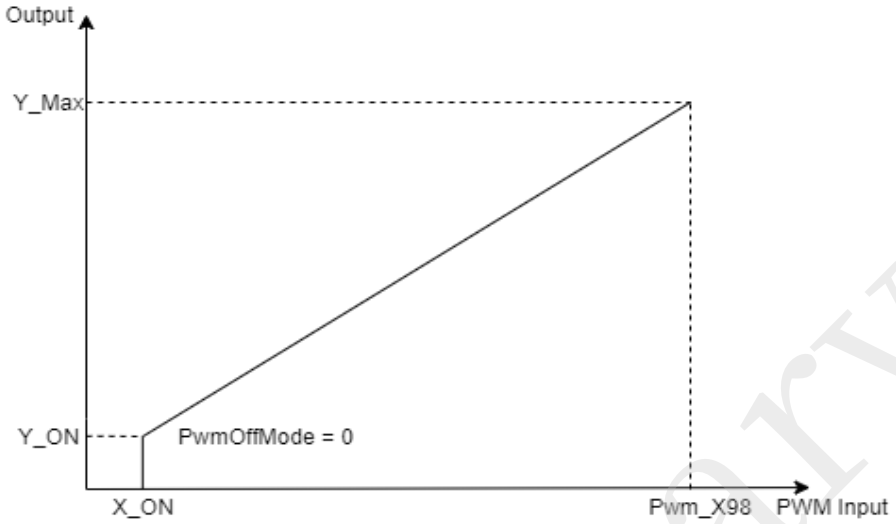


Figure 5-3 Output Curve in Speed/Current/Power Control Mode (PwmOffMode = 0)

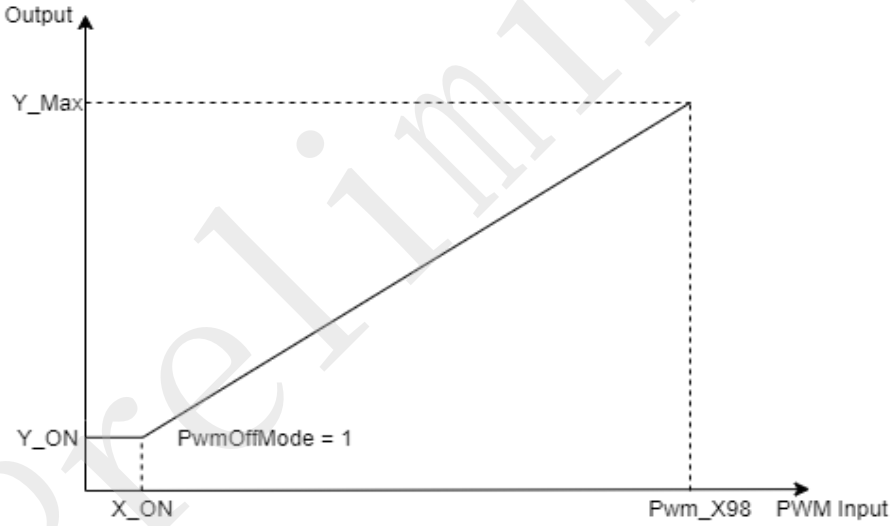


Figure 5-4 Output Curve in Speed/Current/Power Control Mode (PwmOffMode = 1)

5.9 Leading Angle Curve

When Hall effected SVPWM control is selected, the motor angle used in controller should be compensated to improve the operating efficiency. The compensated leading angle with voltage duty cycle is shown in Figure 5-5. The value of X-axis is the duty cycle of voltage reference and the value of Y-axis is the leading angle. Multi segment leading angle curve is configured by 9 duty cycle points, 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, 87.5% and 100%. The maximum leading angle increment between two adjacent duty cycles is 10.547°.

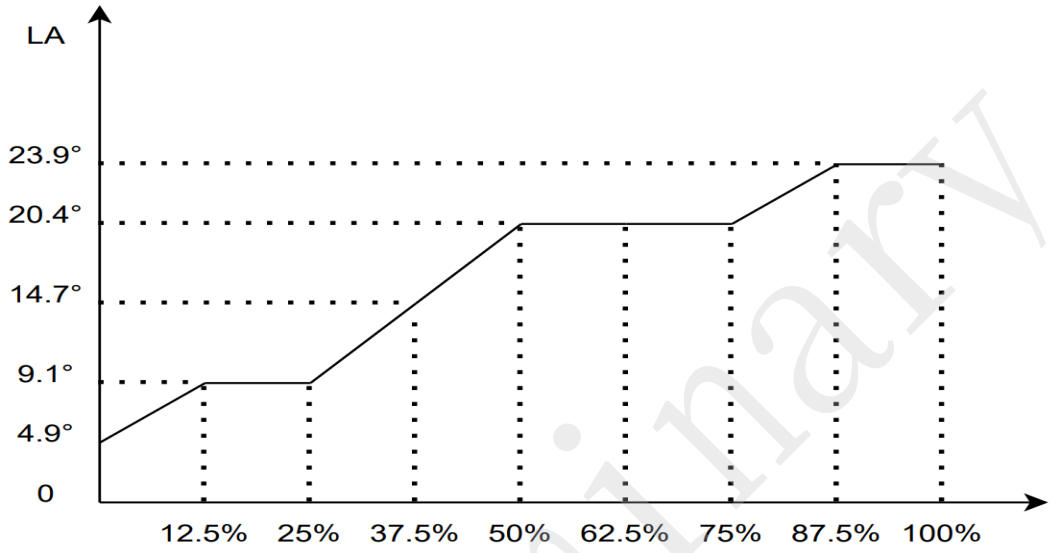


Figure 5-5 Leading Angle Curve

5.10 Sleep Mode

The chip will work in sleep mode when motor is in stop state for 6 seconds.

Wake up:

- I2C interface mode: The chip is awakened after receiving the matched I2C ID
- PWM & CLOCK mode: When the input reverse function is disabled, the chip is awakened after SPEED receiving high level. When the input reverse function is enabled, the chip is awakened after SPEED receiving low level.
- Analog voltage mode: The chip is awakened when the voltage of ASPEED is bigger than 1.5V or the input of SPEED is high level

5.11 Soft-On, Soft-Off

Soft-On function gradually increases the current during the start-up process. Soft-off function gradually reduces the current during the shutdown process. This function can reduce motor noise and make the start-up and shutdown process smoothly.

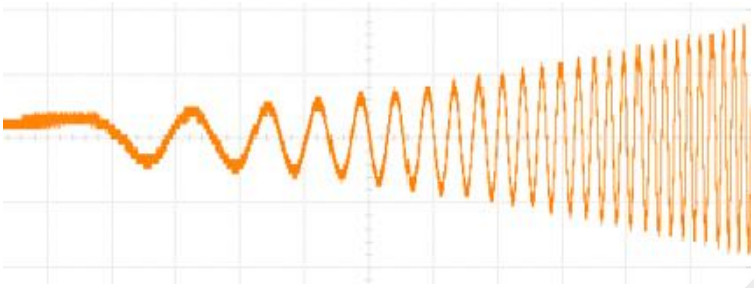


Figure 5-6 Soft-On Phase Current Wave

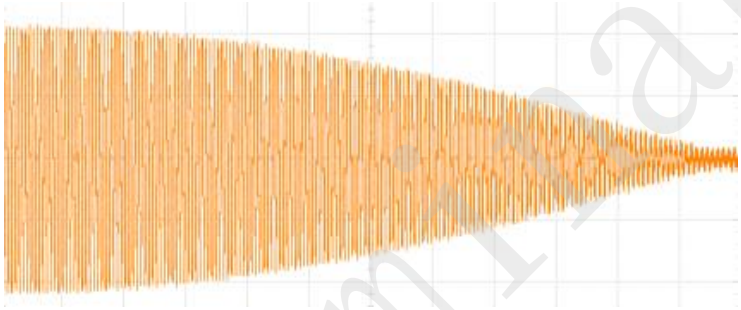


Figure 5-7 Soft-Off Phase Current Wave

5.12 Lock Protection

Lock protection circuitry monitor motor operating state. When locked rotor condition is detected, the chip will turn off output and restart motor, according to the configuration, after 6 seconds.

5.13 Phase Loss Protection

Phase loss protection circuitry monitor motor operating state. When Phase loss condition is detected, the chip will turn off output and restart motor, according to the configuration, after 6 seconds.

5.14 Overcurrent Protection

When the sampling current is larger than overcurrent threshold, the chip will turn off output and restart motor, according to the configuration, after 6 seconds.

5.15 Frequency Multiplication and Division of FG

When FG function is enabled, FG/RD pin is used to output FG signal. The output frequency of FG signal is configured by FGDIV and FGMUL. FGMUL can be configured as 1, 2, 3 or 4. FGDIV can be configured as 1, 1/3, 1/4 or 1/5. k is FG output frequency coefficient and k = FGMUL*FGDIV.

Table 5-1 The Configuration of k

Coefficient k		FGMUL			
		1	2	3	4
FGDIV	1	1	2	3	4
	1/3	1/3	2/3	3/3	4/3
	1/4	1/4	2/4	3/4	4/4
	1/5	1/5	2/5	3/5	4/5

Numbers of FG signal in a mechanical cycle is pp*k, where pp is the pole pairs of motor.

E.g., to generate 3 FG signal in a mechanical cycle for a 4 pole pairs motor, set FGMUL to 3, set FGDIV to 1/4 and k = 3/4.

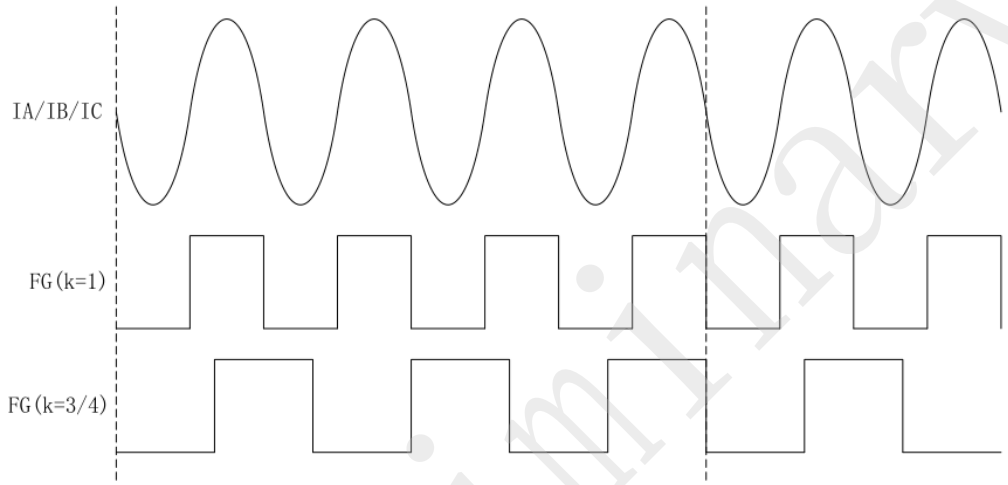


Figure 5-8 FG Output Waveforms When k = 1 and k = 3/4

In Hall effected mode, FG triple frequency or FG base frequency following mode is configurable. The chip output FG signal based on the configured frequency. If FG following function is disabled, the chip output FG signal based on the configuration of FGMUL and FGDIV.

5.16 CLOCK Speed Regulation Mode

In CLOCK speed regulation mode, SPEED is the input of PWM frequency reference. The speed reference is controlled by PWM frequency reference. FGMUL and FGDIV are used to set the factor between speed reference and PWM frequency reference. Speed reference = (PWM frequency reference *60/pp)/(FGMUL*FGDIV).

E.g., providing motor is 5 pole pairs, FGMUL is set to 2, FGDIV is set to 1/3 and the PWM frequency reference is 100Hz, k = 2/3 and speed reference = (100Hz *60/5)/(2/3) = 1800rpm.

6 Document Change List

Date	Revision	Changes
2022/01/04	V0.1	Document pre-publishing
2022/02/09	V0.1	Correct some typos
2022/2/23	V0.2	Add FT8132S SSOP24 related information
2022/03/03	V0.2	Change unit from nS to ns Modify the description of FG/RD part Modify the description of ports EU,EV,EW Modify the description of Overview and Features Modify 8132S Package Size table
2022/03/27	V0.3	Document format standardizing
2022/04/15	V0.4	Document format standardizing and minor content update
2022/06/09	V0.5	Minor content and format update

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