Datasheet

600V Half-bridge Gate Driver

FD2606S

Fortior Technology (Shenzhen) Co., Ltd.

Content

FD2606S 600V Half-bridge Gate Driver

1 System Introduction

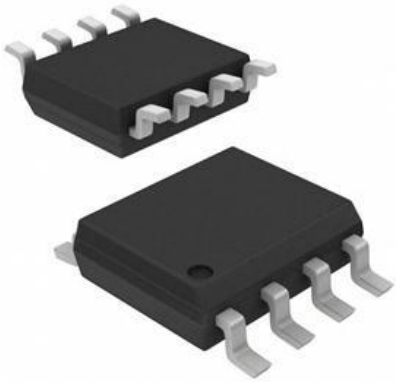
1.1 Overview

FD2606S is a high-voltage and high-speed half-bridge gate driver. It can drive N-type power MOSFETs and IGBTs.

FD2606S has also built-in VCC and VB undervoltage (UVLO) protection to prevent the power semiconductor devices from operation under very low voltage.

FD2606S logic input is compatible with TTL and CMOS (down to 3.3V) for easy interface with control devices. The driver outputs a high pulse current buffer designed with the best driver transconductance.

1.2 Package



SOP8

1.3 Features

- Suspension absolute voltage +600V
- Power supply pressure range: 10V~20V
- 3.5V/5V input logic compatible
- VCC/VBS undervoltage protection (UVLO)
- Output is in phase with the input
- Cross-conduction prevention logic
- Built-in dead time
- High and low channel matching
- RoHS compliant

1.4 Applications

- Motor drives
- DC-AC inverter drives

1.5 Functional Block Diagram

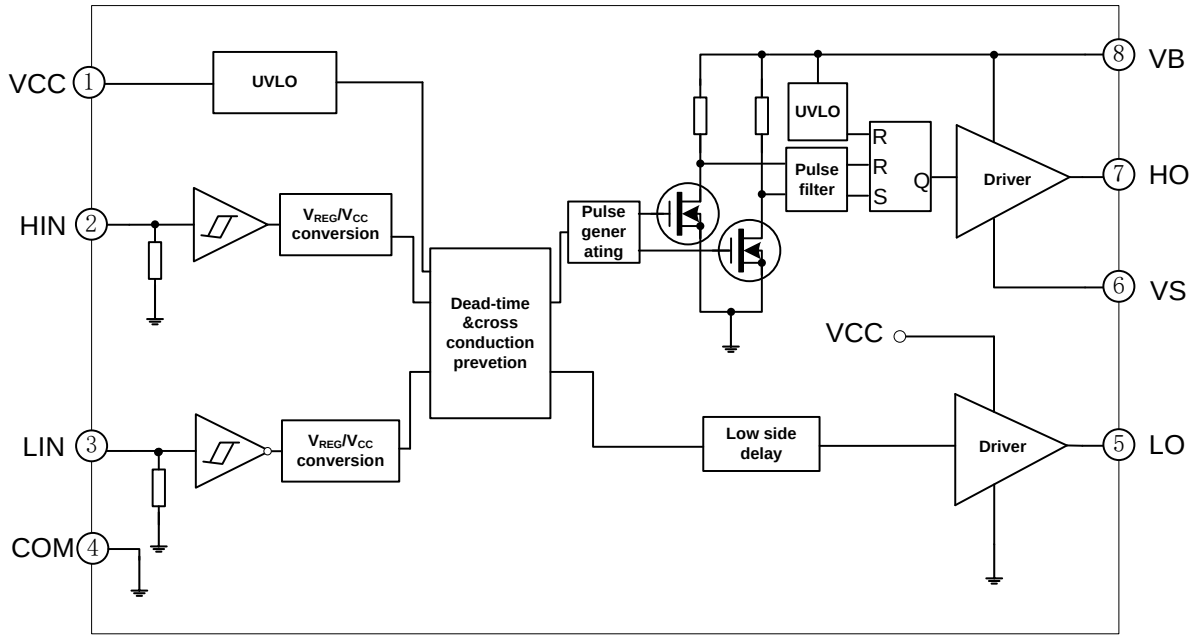


Figure 1-1 Functional Block Diagram of FD2606S

1.6 Pin Diagram

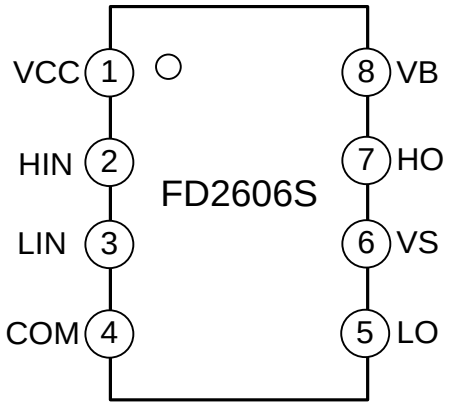


Figure 1-2 Pin Diagram of FD2606S

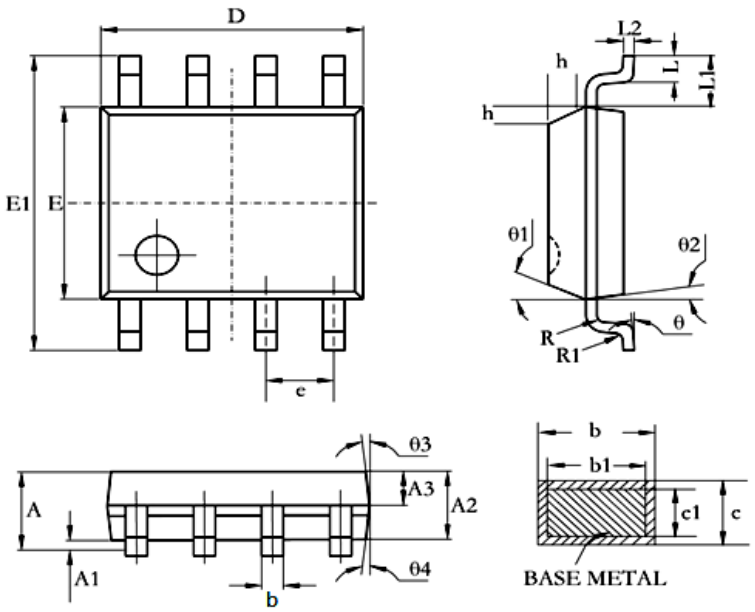
1.7 Pin Definitions

Table 1-1 FD2606S Pin Descriptions

Pin No.	Pin Name	Pin Description
1	VCC	Low-side supply voltage
2	HIN	High-side input
3	LIN	Low-side input
4	COM	Ground
5	LO	Low-side output
6	VS	High-side floating offset voltage
7	HO	High-side output
8	VB	High-side float absolute voltage

2 Package Information

2.1 FD2606S SOIC-8



Symbol	Dimensions in mm			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.36	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.25	1.40	1.65	0.049	0.055	0.065
A3	0.50	0.60	0.70	0.020	0.024	0.028
b	0.38	-	0.51	0.015	-	0.020
b1	0.37	0.42	0.47	0.015	0.017	0.019
c	0.17	-	0.25	0.007	-	0.010
c1	0.17	0.20	0.23	0.007	0.008	0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	5.80	6.00	6.20	0.228	0.236	0.244
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC					
L	0.45	0.60	0.80	0.018	0.024	0.031
L1	1.04REF					
L2	0.25BSC					
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
h	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	-	8°	0°	-	8°
θ1	15°	17°	19°	15°	17°	19°
θ2	11°	13°	15°	11°	13°	15°
θ3	15°	17°	19°	15°	17°	19°
θ4	11°	13°	15°	11°	13°	15°

Product Number	Package Type	Marking ID	Package Method	Quantity
FD2606S	SOP8	FD2606S	Tape & Reel	3000

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

(All pins are referenced to COM unless otherwise specified)

Parameter	Symbol	Min.~Max.	Units
High-side Floating Absolute Voltage	V_B	-0.3～625	V
High-side Floating Offset	V_S	V_B-25～V_B+0.3	V
High-side Output Voltage	V_{HO}	V_S -0.3～V_B +0.3	V
Low-side Supply Voltage	V_{CC}	-0.3～25	V
Low-side Output Voltage	V_{LO}	-0.5～V_{CC}+0.3	V
Logic Input Voltage (HIN, LIN)	V_{IN}	-0.5～V_{CC}+0.3	V
Offset Voltage Slew Rate Range	dV_S/dt	≤50	V/ns
Power Dissipation @T_A≤25°C	P_D	≤0.625	W
Thermal Resistance, Junction to Ambient	R_{thJA}	≤200	°C/W
Junction Temperature	T_j	≤150	°C
Storage Temperature	T_{stg}	-55～150	°C

Notes:

(1) In any case, power dissipation should not exceed P_D.

(2) Voltages above the absolute maximum ratings may damage the chip.

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

(All voltages are referenced to COM unless otherwise specified)

Parameter	Symbol	Min.	Max.	Units
High-side Float Absolute Voltage	V_B	V_S+10	V_S+20	V
High-side Floating Offset Voltage	V_S	Note (1)	600	V
High-side Output Voltage	V_{HO}	V_S	V_B	V
Low-side Supply Voltage	V_{CC}	10	20	V
Low side Output Voltage	V_{LO}	0	V_{CC}	V
Logic Input Voltage (HIN, LIN)	V_{IN}	0	V_{CC}	V
Environment Temperature	T_A	-40	125	°C

Notes:

(1) Logic operational for VS of (COM – 5V) to (COM + 600V). Logic state held for VS of (COM – 5V) to (COM –VBS).

(2) The long-term operation of the chip outside the recommended conditions may affect its reliability. It is not recommended to work in an environment that exceeds the recommended conditions.

3.3 Static Electrical Characteristics

Table 3-3 Static Electrical Characteristics

[V_{BIAS} (V_{CC}, V_{BS}) =15V and T_A =25°C unless otherwise specified.

All the parameters are referenced to COM.]

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Logic "1" Input Voltage	V_{IH}		2.7	-	-	V
Logic "0" Input Voltage	V_{IL}		-	-	0.8	
High-level Output Voltage, V_{BIAS} - V_O	V_{OH}	I_O=20mA	-	0.7	1.2	
Low-level Output Voltage, V_O	V_{OL}		-	0.24	0.4	
Offset Supply Leakage Current	I_{LK}	V_B =V_S =600V	-	1.0	5.0	uA
Quiescent V_{BS} Supply Current	I_{QBS}	V_{IN} =0V or 5V	-	75	120	
Quiescent V_{CC} Supply Current	I_{QCC}		-	160	300	
Logic "1" Input Bias Current	I_{IN+}	V_{IN}=5V	-	25	50	
Logic "0" Input Bias Current	I_{IN-}	V_{IN}=0V	-	-	1	
V_{CC} and V_{BS} Supply Undervoltage Positive Going Threshold	V_{CCUV+} V_{BSUV+}		7.9	8.8	9.7	V
V_{CC} and V_{BS} Supply Undervoltage Negative Going Threshold	V_{CCUV-} V_{BSUV-}		7.2	8.0	8.8	
V_{CC} and V_{BS} Supply Under-Voltage Lock-out Hysteresis	V_{CCUVH} V_{BSUVH}		0.4	0.8	-	
Output High Short Circuit Pulsed Current	I_{O+}	V_O=0V,PW≤10us	130	210	-	mA
Output Low Short Circuit Pulsed Current	I_{O-}	V_O=15V,PW≤10us	230	360	-	

3.4 Dynamic Electrical Characteristics

Table 3-4 Dynamic Electrical Characteristics

(T_A =25°C, V_{CC}=V_{BS}=15V, C_L=1000pF and V_S=COM unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Rising Edge Transmission Time	t_{on}	V_S=0V	--	140	220	ns
Output Falling Edge Transmission Time	t_{off}	V_S=600V	--	140	220	ns
High-low Side Delay Match	MT		--	0	50	ns
Output Rising Time	t_r		--	100	160	ns
Output Falling Time	t_f		--	60	100	ns
Dead-time	DT		--	470	650	ns

4 Typical Application Diagram

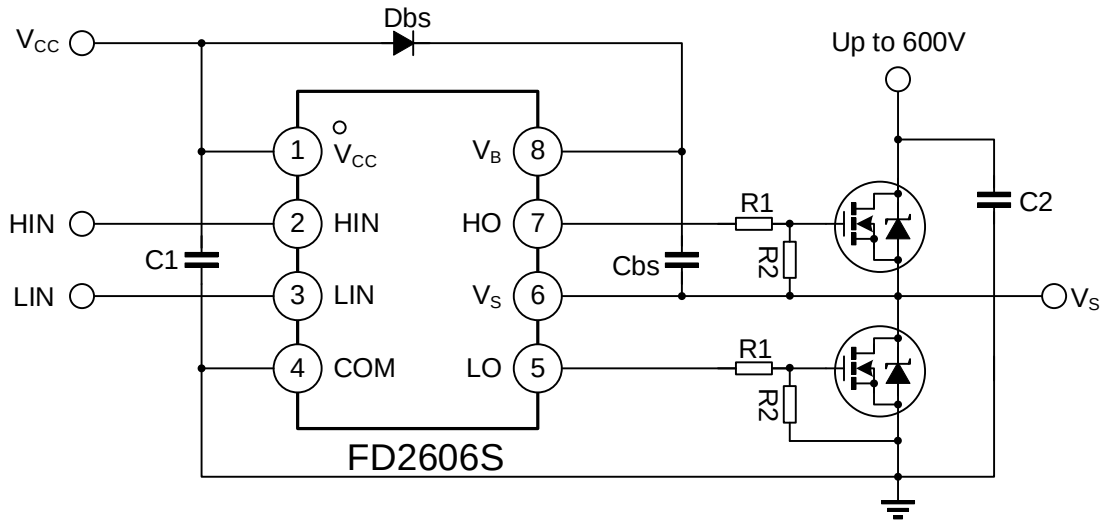


Figure 4-1 Typical Application Diagram of FD2606S

C1: Power filter capacitor, according to the circuit can choose 1μF ~ 10μF, as close to the chip pin as possible.

R1: Gate drive resistor, and the resistance depends on the device being driven.

R2: MOS gate and source resistance.

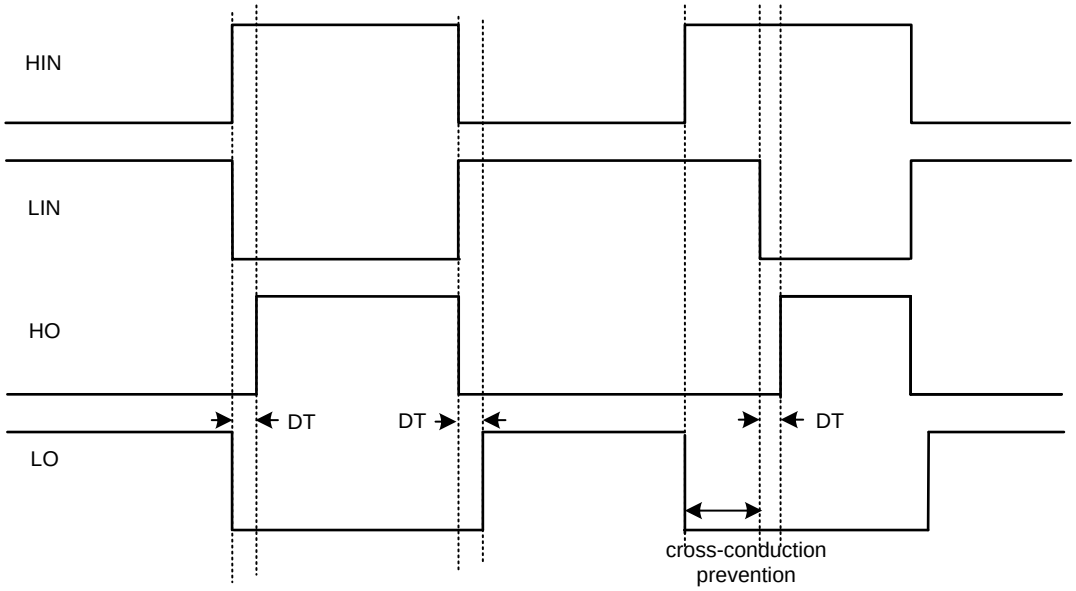
Dbs: Bootstrap diodes. It should be selected for high reverse breakdown voltage Schottky diodes.

Cbs: Bootstrap capacitors. Ceramic capacitors or tantalum capacitors should be selected, according to the circuit can choose 0.22μF ~ 10μF. The capacitor should be as close as possible to the chip pin.

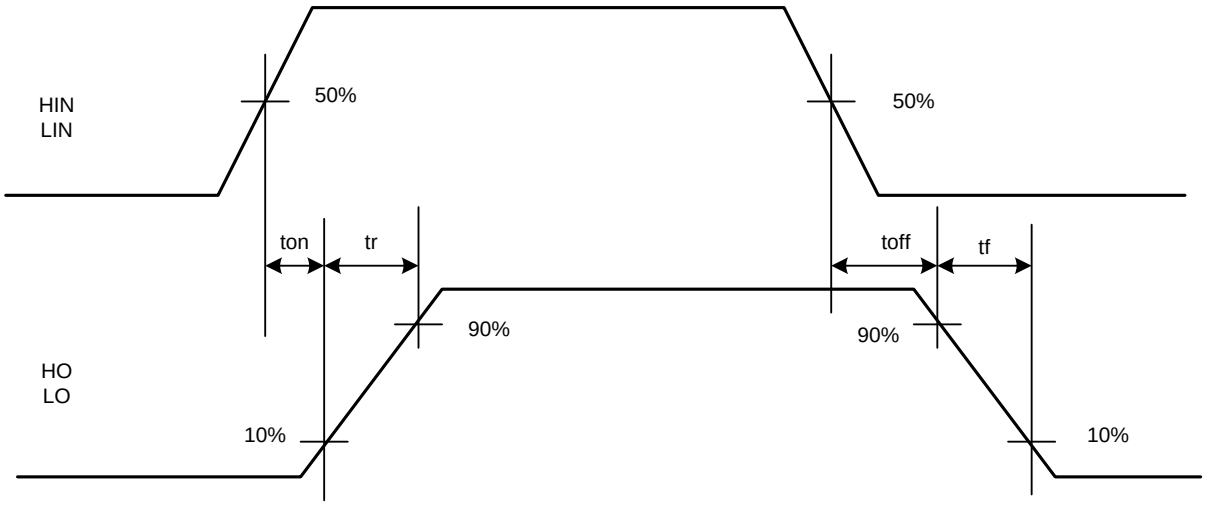
Note:

The above circuits and parameters are for reference only. The actual application circuit should be designed with the measured results in setting the parameters.

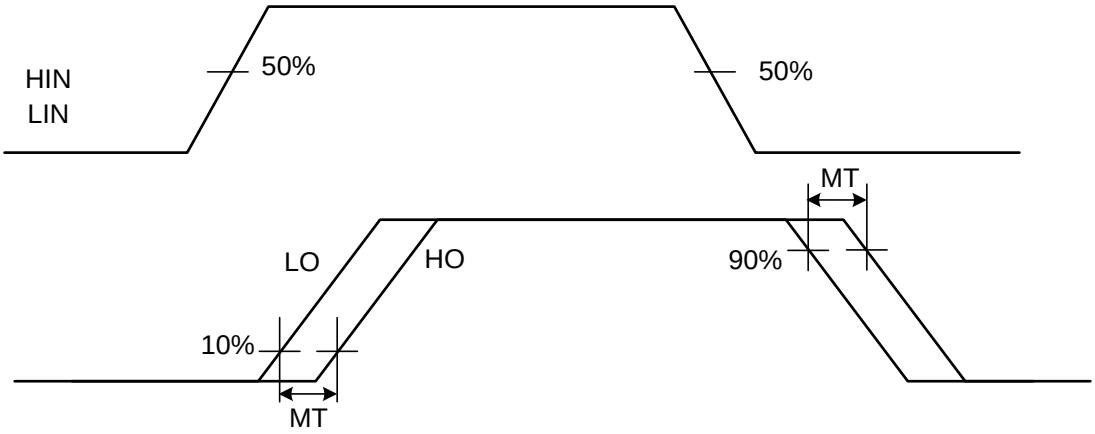
5 Logic Timing Diagram



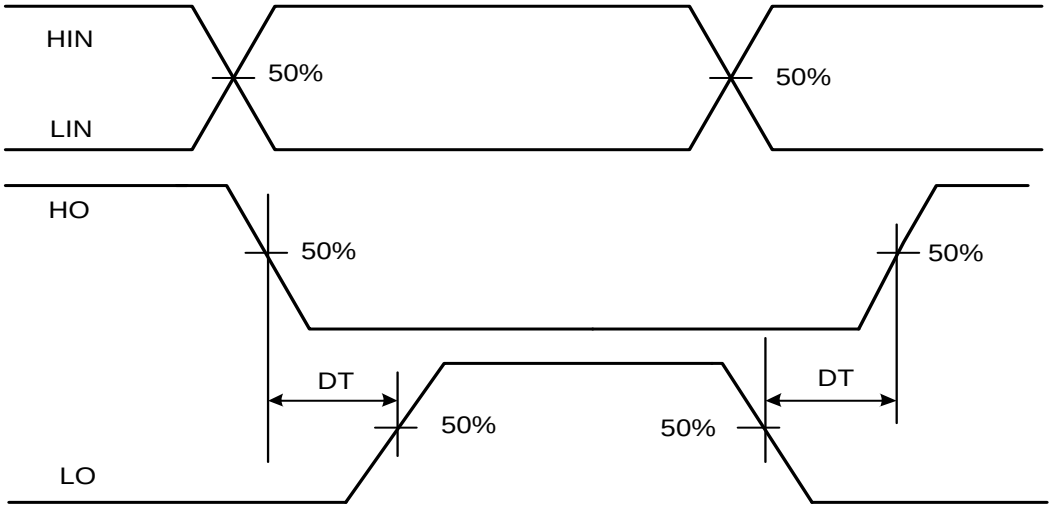
6 Switching Time Test Standards



7 Transmission Time Matching Test Standards



8 Dead-time Test Standards



9 Revision History

Rev.	Descriptions	Date	Prepared By
V0.1	First release.	2019/01/22	Raymond Xie
V1.0	1. Added the resistance R2 in Typical Application Diagram; 2. Corrected some word spellings; 3. Standardized document format.	2023/04/24	Lay Ye / Eric Deng

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Fortior Technology (Shenzhen) Co., Ltd.
Room 203, 2/F, Building No.11, Keji Central Road 2,
Software Park, High-Tech Industrial Park, Shenzhen, P.R. China 518057
Tel: 0755-26867710
Fax: 0755-26867715
URL: http://www.fortiortech.com