# Datasheet

# FT3206N Three-phase Sine-wave Sensorless Motor Drive

Fortior Technology (Shenzhen) Co., Ltd.

Content

# 1 System Introduction

## 1.1 Overview

FT3206N is a three-phase sensorless brushless DC motor driver IC designed for low noise and low voltage applications. It drives the motor sinusoidally, giving low noise performance. It provides such features as start-up circuit, Pulse Width Modulation (PWM) speed control and RD\FG output for different control applications, as well as protective mechanisms including lock protection and thermal protection. FT3206N is especially suitable for silent applications such as game consoles or CPU fans. It is available in DFN3x3-10 package.

FT3206N integrates a wide range of protection features, including lock protection and automatic recovery, thermal shutdown, etc. These prevent the control circuits and the motor from being damaged, particularly under stressed applications and demanding environments.

## 1.2 Applications

NB fans; Masks etc.

## 1.3 Features

- Three-phase Sine-wave Drive
- Three-Phase Sensorless Drive
- Built-In External PWM Speed Control
- FG (Rotation Speed Detection) Output
- RD (Rotation Detection) Output
- Soft Switching Circuit (for noise reduction)
- Power Saving (when input PWM duty cycle is 0%)
- Built-In Lock Protection and Auto Restart
- Built-in Thermal Shutdown Protection (TSD)
- FG Division for Different Pole Paired Motors
- I2C Interface for Parameter Settings and Internal OTP Writing
- Low Rds (0.7Ω)

## 1.4 Functional Block Diagram

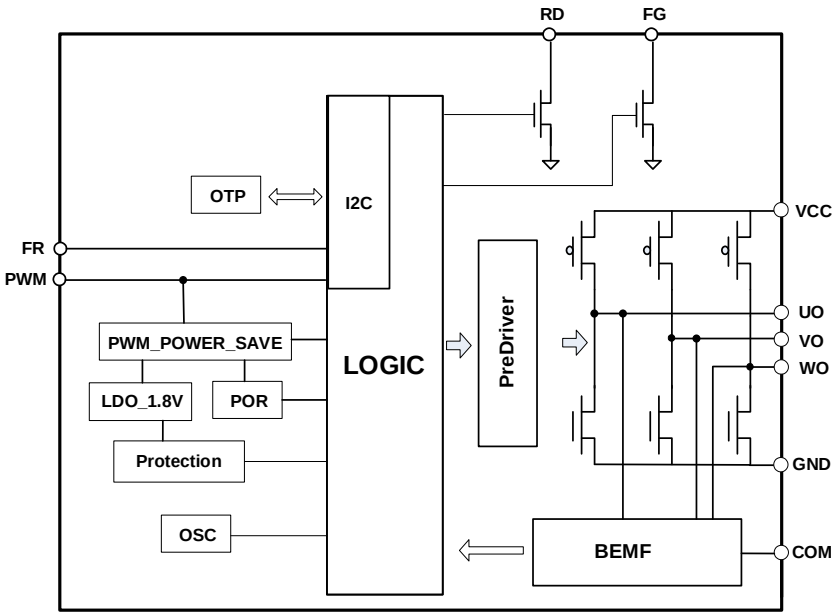
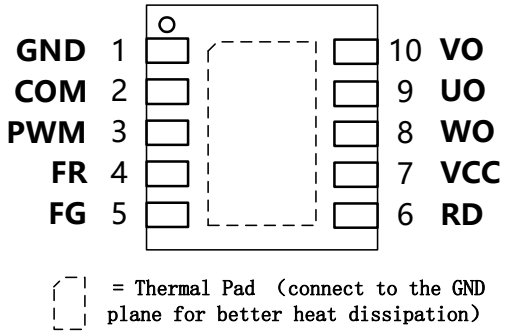



Figure 1-1 Functional Block Diagram of FT3206N

## 1.5 Pinout Diagram

### 1.5.1 FT3206N Pinout Diagram




## 1.6 Pin Definitions

The I/O types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analogue Input
- AO = Analogue Output
- P = Power Supply

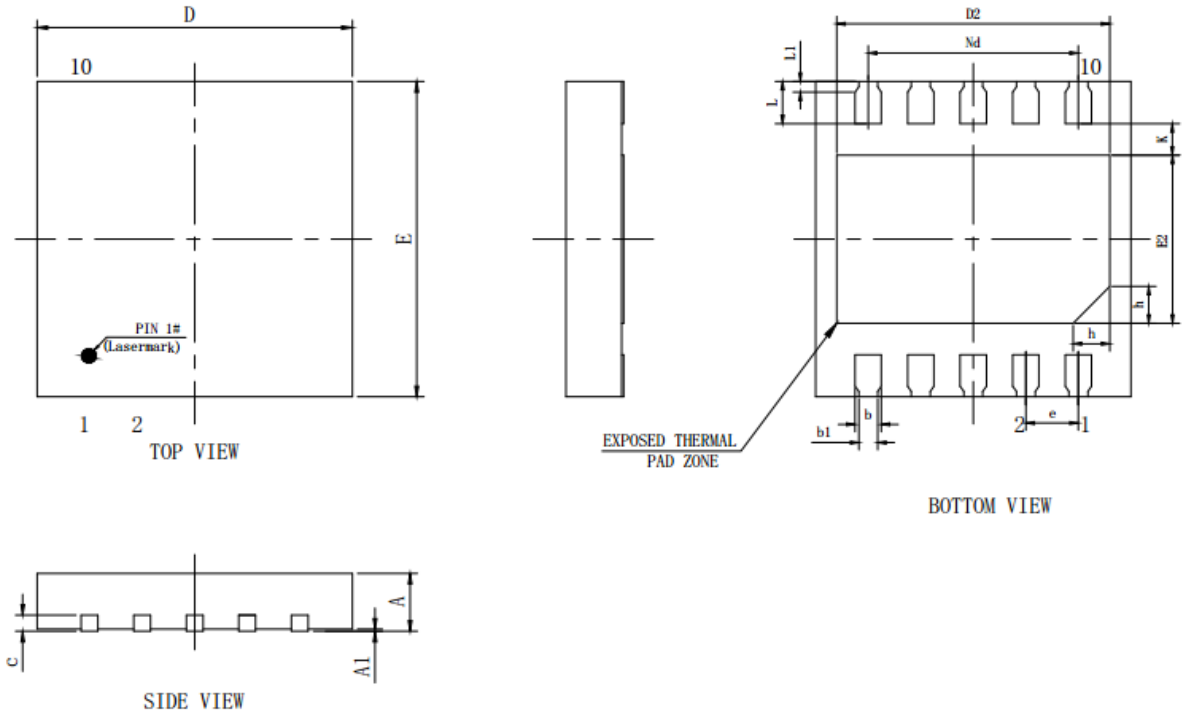
### 1.6.1 FT3206N Pins

Table 1-1 FT3206N Pin Descriptions

| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | GND | GND | Ground Pin |
| 2 | COM | I | Motor Neutral Point Input Pin |
| 3 | PWM | I | PWM Signal Input Pin. Input PWM signal to control rotation speed |
| 4 | FR | I | Motor Spin Direction Control Pin |
| 5 | FG | O | Rotation Speed Output |
| 6 | RD | O | Rotation Detection Output |
| 7 | VCC | POWER | Supply Voltage Input Pin |
| 8 | WO | O | Driver Output Pin. Output signal for driving motor phase W |
| 9 | UO | O | Driver Output Pin. Output signal for driving motor phase U |
| 10 | VO | O | Driver Output Pin. Output signal for driving motor phase V |

## 2 Package Information

### 2.1 DFN10 (3x3mm)




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0. 50 | 0.55 | 0. 60 |
| A1 | 0 | 0.02 | 0. 05 |
| b | 0. 20 | 0. 25 | 0. 30 |
| b1 | 0. 18REF | | |
| c | 0. 152REF | | |
| D | 2. 90 | 3. 00 | 3. 10 |
| D2 | 2. 50 | 2. 60 | 2. 70 |
| Nd | 2. 00BSC | | |
| E | 2. 90 | 3. 00 | 3. 10 |
| E2 | 1. 50 | 1. 60 | 1. 70 |
| e | 0. 50BSC | | |
| K | 0. 25 | 0. 30 | 0. 35 |
| L | 0. 35 | 0. 40 | 0. 45 |
| L1 | 0. 10REF | | |
| h | 0. 30 | 0. 35 | 0. 40 |

Figure 2-1 DFN10 Package Outline Dimensions

| Part Number | Package Type | Marking ID | Package Method | Quantity |
|---|---|---|---|---|
| FT3206N | DFN10 | FT3206N | Tray | 490 |

## 3 Ordering Information

Table 3-1 Model Options

| Type | Package | Power Supply (V) | Rdson (High side + low side) | Bus Current Average Value (A) | Control Functions | | | | | | Protection | | | | | Operation Temperature $T_j$ (°C) | Lead-free |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Driver Method | Speed Regulation Mode | | | Forward and Reverse Rotation | Initial Position Detection | Over-current Protection | Over-temperature Protection | Under-voltage Protection | Lock Protection | Phase Loss Protection | | |
| | | | | | | I2C | PWM/CLOCK | Analog Input | | | | | | | | | |
| FT3206N | QFN10 (3x3 mm) | 2-6 | 0.7 | 0.5 | Sensorless SVPWM | - | √ | - | √ | - | - | √ | √ | √ | - | -40~150 | √ |

# 4 Electrical Characteristics

## 4.1 Absolute Maximum Ratings

Stresses exceeding the "Absolute Maximum Ratings" listed in Table 4-1 Absolute Maximum Ratings may cause irremediable damages to the device. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability. It is not recommended to use the stresses above the Absolute Maximum Ratings for the design.

Table 4-1 Absolute Maximum Ratings

($T_A$ = 25°C unless otherwise specified)

| Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage (VCC max.) | | - | - | 7 | V |
| VCC Current ($I_{VCC}$ max.) | | - | - | 1 | A |
| Driver Output Pin Withstand Voltage ($V_{mot}$ max.) | | - | - | 7 | V |
| Logic Input Pin Withstand Voltage ($V_{logic}$ max.) | | - | - | 7 | V |
| RD/FG Output Pin Withstand Voltage (VRD/FG max.) | | - | - | 7 | V |
| RD/FG Output Current (IRD/FG max.) | | - | - | 10 | mA |
| Junction Temperature ($T_J$) | | -40 | - | 150 | ℃ |
| Operating Temperature ($T_{opr}$) | | -40 | - | 105 | ℃ |
| Storage Temperature ($T_{stg}$) | | -65 | - | 150 | ℃ |
| Thermal Resistance-Junction to Ambient [1] ($\theta_{JA}$) | | - | 93 | - | ℃/W |
| Thermal Resistance-Junction to Case [2] ($\theta_{JC}$) | | - | 42 | - | ℃/W |

Notes:

(1) $\theta_{JA}$ is measured with the component mounted on a 76.2mm × 114.3mm × 1.6mm glass epoxy board (one-layer) in free air.

(2) The junction-to-case thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in ANSI SEMI standard G30-88.

## 4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

| Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage (VCC) | | 2 | - | 6 | V |
| VCC Current ($I_{VCC}$) | VCC Average Output Current | - | - | 500 | mA |

## 4.3 Global Electrical Characteristics

Table 4-3 Global Electrical Characteristics

($T_A$ = 25°C and VCC = 5V unless otherwise specified)

| Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VCC Operating Current ($I_{vcc\text{-}work}$) | Working Current | - | 5 | - | mA |
| VCC Sleep Current ($I_{vcc\text{-}sleep}$) | Sleep Current | - | 100 | - | μA |
| **Output Block** | | | | | |
| High-side Switch ON Resistance Ron (H) | $I_O$ = 0.5A | - | 0.4 | 0.7 | Ω |
| Low-side Switch ON Resistance Ron (L) | $I_O$ = 0.5A | - | 0.3 | 0.5 | Ω |
| **Digital I/O Section — PWM, FR** | | | | | |
| Digital High-level Input Voltage ($V_{dinh}$) | - | 3.0 | - | VCC+ 0.3 | V |
| Digital Low-level Input Voltage ($V_{dinl}$) | - | -0.3 | - | 0.8 | V |
| PWM High Input Current ($I_{PWMH}$) | PWM = VCC | - | 0 | - | μA |
| PWM Low Input Current ($I_{PWML}$) | PWM = GND | - | 7 | - | μA |
| Digital I/O Internal Pull-up Resistor ($R_{dio}$) | - | - | 70k | - | ohm |
| PWM Input Frequency ($F_{PWM}$) | | 1 | - | 50 | kHz |
| **RD/FG Output Pin** | | | | | |
| RD/FG Output Low-level Voltage ($V_{RDFG}$) | When $I_O$ = 5 mA | - | 0.1 | 0.2 | V |
| **Lock Protection** [1] | | | | | |
| Lock Detection On Time ($T_{ON}$) | When RSF = 54, Ton = 6 | - | 0.94 | - | s |
| Lock Detection Off Time ($T_{OFF}$) | | - | 5 | - | s |
| **Thermal Protection Circuit** | | | | | |
| Thermal Protection Circuit Operating Temperature (TSD) | Design target | - | 165 | - | ℃ |
| Temperature Hysteresis Width (ΔTSD) | Design target | - | 30 | - | ℃ |

Notes:

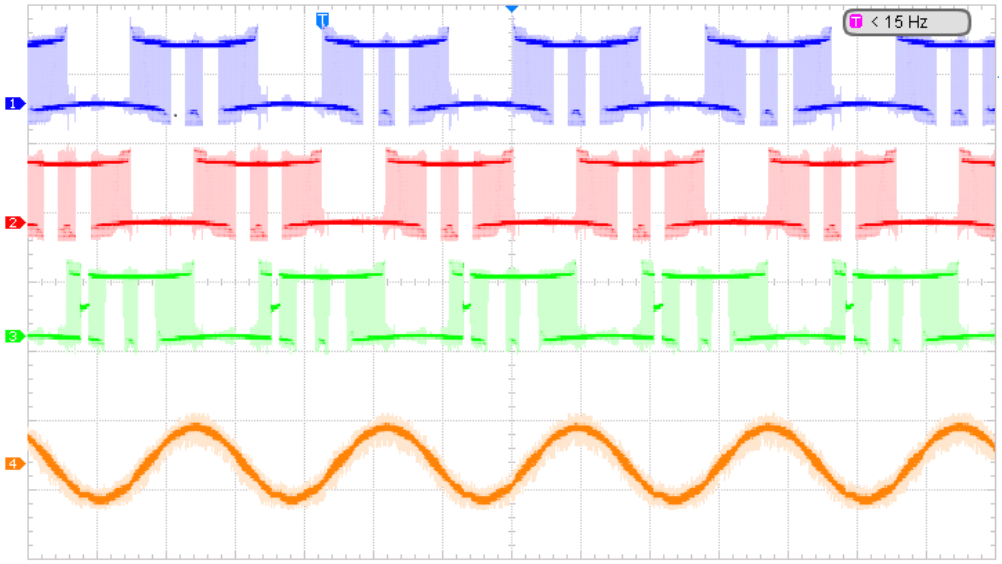
(1) Lock detection time is configurable by using UI setting. $T_{ON}$ can be set from 0.1s to 7s.

(2) Initial Speed Detection is enabled or disabled based on UI setting.

(3) The chip enters sleep mode when the external input PWM with 0% duty cycle lasts for 8ms.

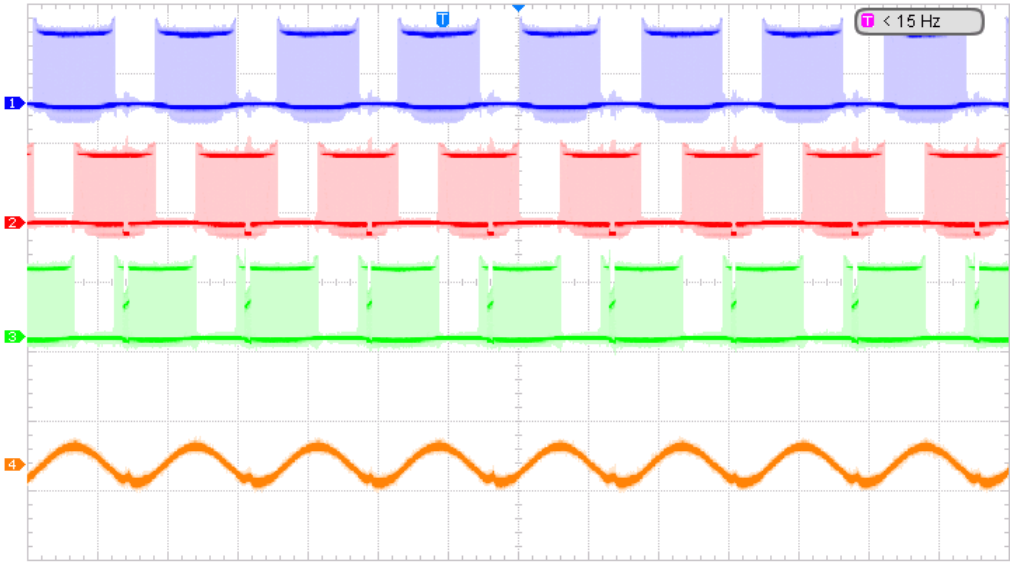
# 5 Operating Waveforms

## 5.1 Rotation Waveform (PWM = 100%)




- CH1: $V_{UO}$, 5V/div, DC
- CH2: $V_{VO}$, 5V/div, DC
- CH3: $V_{WO}$, 5V/div, DC
- CH4: $I_{UO}$, 200mA/div, DC

## 5.2 Rotation Waveform (PWM = 50%)




- CH1: $V_{UO}$, 5V/div, DC
- CH2: $V_{VO}$, 5V/div, DC
- CH3: $V_{WO}$, 5V/div, DC
- CH4: $I_{UO}$, 200mA/div, DC

# 6 Function Descriptions

Please read the following notes before designing driver circuits with FT3206N.

## 6.1 Starting

Starting of the motor is triggered by the detection of PWM signal. The IC injects a configurable starting commutation frequency to the motor. During this commutation, BLDC drive is used so as to detect back-EMF from the silent windows. After the IC has detected a stable back-EMF, it transits to SINE drive.

## 6.2 Dual Start

The IC adopts a strategy of dual starting. The IC is injected with a configurable commutable frequency for back-EMF detection. If a stable back-EMF is detected, it transits to SINE drive. If a unstable back-EMF is detected, the starting sequence is immediately restarted, providing a consecutive/extended starting commutation, aiming to increase and improve the stability of the starting back-EMF

## 6.3 PWM Speed Control

The IC accepts a wide range of PWM input frequency from 1kHz to 50kHz for motor speed control. The input PWM is translated to an output PWM fixed at a frequency of 30kHz, away from the audible frequency range.

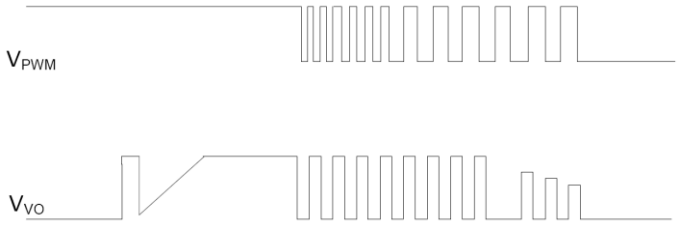



Figure 6-1 PWM Input Waveform

## 6.4 Pseudo-sine Output

The IC switches from BLDC to PSEUDO-SINE output after the back-EMF signals are stable. Under PSEUDO-SINE drive, the IC opens only a window for back-EMF detection while the rest of the cycle is driven sinusoidally. For the realization of the sine drive, SVPWM is being used.

## 6.5 FG Output

The FG pin is configurable to different multiples of the electrical motor frequency to accommodate for different pole paired motors. A square wave signal is provided to the open-drain output. Being an open-drain, a pull-up resistor is necessary for proper operation of the output.

## 6.6 Lock Protection and Automatic Recovery

The IC is designed with lock protection and configurable recovery feature for both motor and IC

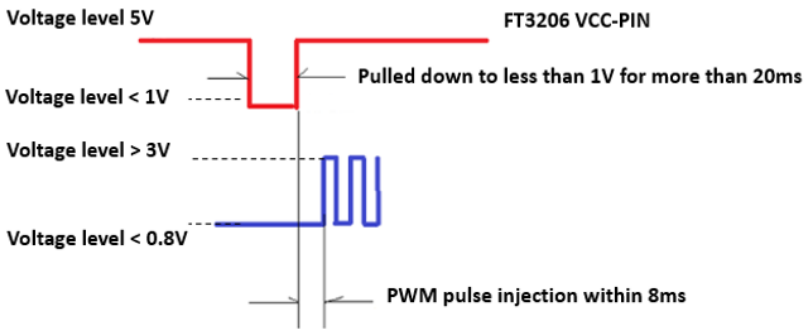
protection. Upon detection of a lock condition or a detached motor terminal condition, the IC enters a gate turn-off condition, which lasts for 5secs before the IC is re-started. The number of times of re-starting is configurable to either 0, 1, 3 or 9 depending on application.

### 6.7 Thermal Protection

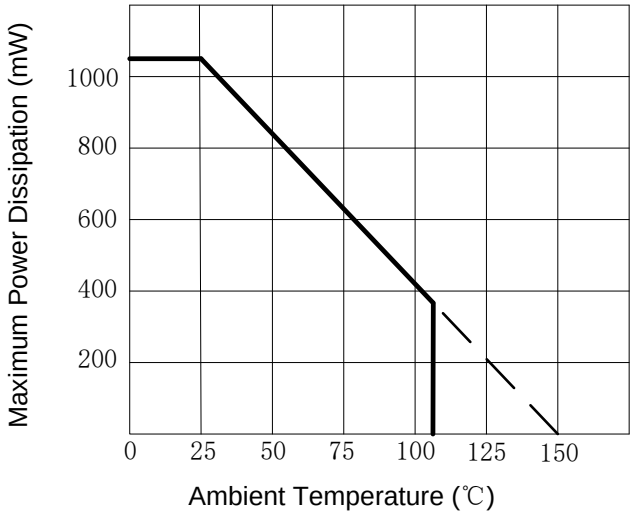
The IC has thermal protection feature. When internal junction temperature reaches 160℃, the IC goes into gate turn-off condition. When the temperature drops to 130℃, the IC performs an internal reboot and commences the starting sequence.

### 6.8 IC Low Power Wake Up Sequence

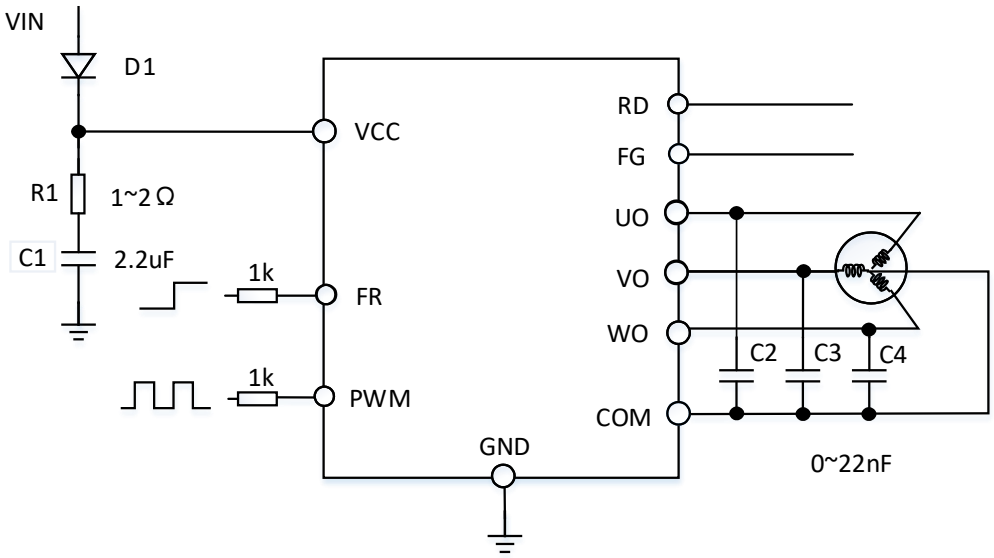
With VCC supplied and PWM pulled low, the IC enters low-power mode. To wake up the IC, VCC must be first pulled to less than 1V for more than 20ms. Upon recovery of VCC to 5V, PWM pulses must be injected within 8ms.




## 7 Maximum Power Dissipation v.s. Ambient Temperature



## 8 Application Circuit Example




Notes

(1) D1 is used to prevent the damage from the power reverse connection.

(2) R1 and C1 are for power supply filtering feature, and must be placed as close to IC as possible.

(3) C2 ~ C4 are optional. It depends on the performances of the motor.

## 9 Revision History

| Rev. | Descriptions | Date | Prepared By |
|---|---|---|---|
| V1.0 | First release | 2020/03/11 | Kun Li |
| V1.1 | 1. Corrected I/O type of RD from "I" to "O" in Table 1-1 FT3206N Pin Descriptions;<br>2. Added section 1.2 Applications;<br>3. Added section 3 Ordering Information;<br>4. Corrected the minimum value of PWM Input Frequency (FPWM) from "0.2kHz" to "1kHz" in Table 4-3 Global Electrical Characteristics;<br>5. Deleted descriptions on Quick Start;<br>6. Added section 6.8 IC Low Power Wake Up Sequence;<br>7. Added "If there are any differences between the Chinese and the English contents, please take the Chinese version as the standard." in Copyright Notice;<br>8. Standardized document format;<br>9. Corrected some grammar mistakes and wrong sentences. | 2023/04/21 | Eric Deng |
| V1.2 | 1. Modified the parameter name "Output Current ($I_{OUT}$ max.)" in Table 4-1 Absolute Maximum Ratings as "VCC Current ($I_{VCC\ max.}$)";<br>2. Modified the parameter name "Output Current ($I_O$)" in Table 4-2 Recommended Operating Conditions as "VCC Current ($I_{VCC}$)", and the test condition "UO/VO/WO Average Output Current" as "VCC Average Output Current";<br>3. Modified the parameter names "Power Supply Current 1 ($I_{CC}1$)" and "Power Supply Current 2 ($I_{CC}2$)" in Table 4-3 Global Electrical Characteristics as "VCC Operating Current ($I_{vcc\text{-}work}$)" and "VCC Sleep Current ($I_{vcc\text{-}sleep}$)", and the test condition "Standby Current" as "Sleep Current"; Added "The chip enters sleep mode when the external input PWM with 0% duty cycle lasts for more than 8ms." to Notes;<br>4. Corrected the range of PWM input frequency in section 6.3 PWM Speed Control from "200Hz to 50kHz" to "1kHz to 50kHz";<br>5. Corrected some wrong words. | 2023/05/12 | Eric Deng |

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